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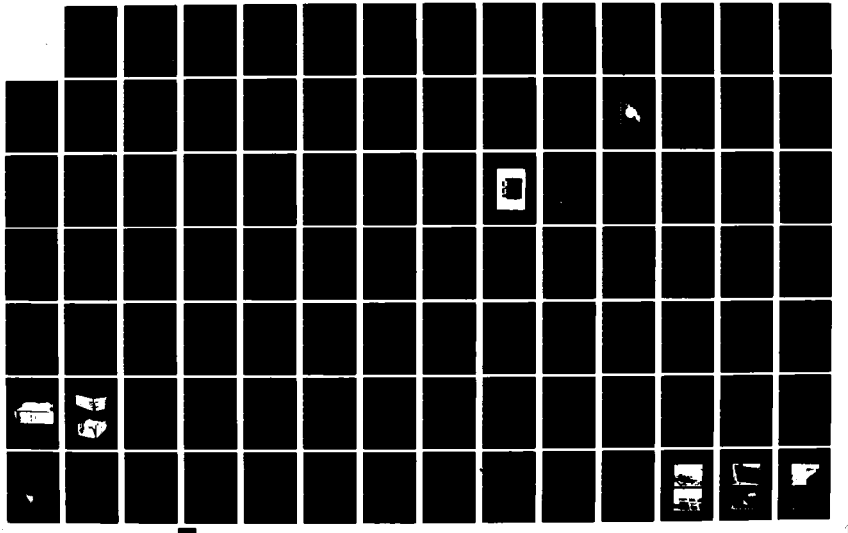

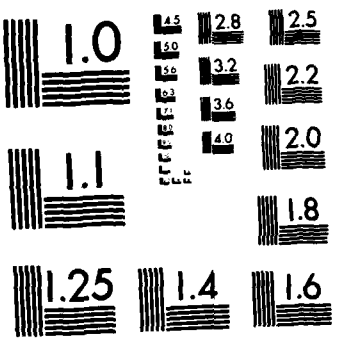

THE FIRST CORTICAL IMPLANT OF A SEMICONDUCTOR MULTIELECTRODE ARRAY: ELECTRODE DEVELOPMENT AND DATA COLLECTION

THESIS

AFIT/GE/EE/82D-29

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Wright-Patterson Air Force Base, Ohio

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THESIS

Presented to the Faculty of the School of Engineering
of the Air Force Institute of Technology,
Air University
in Partial Fulfillment of the
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Master of Science in Electrical Engineering

by

Russell W. Hensley, Capt. USAF
and
David C. Denton, 1st Lt. USAF

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PREFACE

The human visual system is wonderfully complex and mysterious. With apparent ease, it recognizes the written word or familiar faces. Although much is known about the anatomy and structure of the system, the transforms and algorithms used by the human visual system remain unknown. If it were possible for researchers to probe the "inner working of visual cortex", they might better understand visual functions. Ultimately with such a tool the functions of all cortex might be revealed.

Every advancement man has ever made started with one perhaps insignificant step. It is our sincere desire to provide neuro-research with that small step. This research concerns itself with proving that a small semiconductor multielectrode array is that tool which can, at high spatial resolution, effectively and non-destructively examine the bioelectric signals produced by the cortex. Then, with the availability of ample cortical information, others may determine the form of the transforms and algorithms.

We gratefully acknowledge the support of Major John G. Golden, DVM, BSC, Cmsgt William C. Johnson and Ssgt Richard Switzer, the surgical team of the Aerospace Medical Research Laboratory, whose expertise made this implant possible. We also thank Mr Alva Karl for his technical advise.

Our appreciation is extended to Capt Roger Colvin, PhD, Lt Robert Bellacicco, Lt Jayme La Voie and Lt Wilfred Posten for their effort in both the redesign of the multielectrode

array and procurement of a commercial version of the array. Also, Mr Larry Hollatz and the gentlemen of the National Cash Register Company aided significantly in this effort.

We gratefully recognize Mr James Skalski and the Device Technology Group of the Avionics Laboratory for their help in the development and inspection of the multielectrode array.

For their interest and encouragement and for their patience we thank our committee members, Dean L. E. Wolaver and Major Larry Kizer.

We especially thank Dr Matthew Kabrisky for fifteen months of inspiration, guidance and encouragement during this thesis effort.

And equally important, we express our gratitude to our wives and families, Lora and Philip Denton and Rosa, Melissa and Rusty Hensley. For patiently understanding and lovingly enduring long hours of absence and study, we thank you.

David C. Denton

Russell W. Hensley

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ABSTRACT

Previous bioengineering research conducted at the Air Force Institute of Technology (AFIT) motivated the development of a multielectrode array capable of extracting and recording bioelectrical signals present on the mammalian cortex. Part of the work presented here involves the total redesign and packaging of the drive circuitry necessary to operate the AFIT Array. Visual evoked response (VER), independent test circuitry and JFET compensation were also incorporated into the redesign. Several unique packaging techniques were developed to protect the semiconductor devices from a Cerebrospinal Fluid (CSF) (ie. saline) environment. New encapsulation processes with polyimide enabled development of the AFIT Array into a chronic cortically implantable probe. A simple nondestructive surgical procedure was developed, which permits access to visual cortex. The probe was then implanted into a laboratory beagle and bioelectrical (cortical) data were collected over a period of 19 days. VER techniques were used to test whether the biological data collected reflected actual brain functions. The data analysis to date clearly shows the bioelectric signals to be electroencephalographic (EEG) in origin. Conclusions about the AFIT array, encapsulation, drive system, surgical technique and data analysis are discussed. Recommendations for future research with the AFIT Array pertain to most aspects of this experiment. Furthermore, there are recommendations for additional experiments.

CHAPTER I

INTRODUCTION

BACKGROUND

The mammalian brain is the most advanced computing "machine" known and has inspired many attempts to model its functions. Of particular interest are its functions related to visual scene analysis and pattern recognition. Numerous researchers have attempted to model such functions concentrating primarily on visual information processing. Fortunately, the eye-brain system is reasonably accessable, easily distinguished and extensively studied. In fact, a detailed "wiring diagram" exists for the eye-brain system (Ref. 1); but how it performs perception or recognition is as yet unknown.

To date, brain activity has been studied at two primary levels: first, the standard electroencephalograph (EEG) using gross electrodes on the scalp and second, the recording of individual neuron activity via microprobes. Although much has been done to gain an understanding that should lead to an accurate model, such a model has not yet been realized. Attempts at modeling the visual recognition function from data gathered at the EEG level have been compared to modeling a complex computer by simply analyzing its output. At the other extreme, however, building a model based on collected data from one or several neurons individually, may be compared to modeling a computer by

observing the activity of a single component. Each extreme provides important information, but neither has led to a model which explains the integrated eye-brain activity or its visual perception capabilities. Thus, there appears to be a level of brain function and analysis which has not yet been researched. In fact, based upon the fundamental neuroanatomical work of Lorente deNo in the 1930's, a series of investigators including among others, Mountcastle, Kabrisky, Hubel and Wiesel have hypothesized that brain circuitry is arranged into basic computing elements (BCE's) each containing from three hundred to five hundred neurons (Ref. 1,2,3,4). These investigators have together suggested that an analysis of the neuronal interconnection schemes between the BCE's might actually be required to account for the computational capability of the brain. Additional understanding of BCE electrical activity combined with EEG and microprobe data, may then allow an understanding of the scene analysis/recognition functions performed by the brain. An understanding of basic computing element electrical activity requires evaluation of BCE data.

Is it possible to collect simultaneous data from a substantial number of independent, adjacent BCE's? Until this work began such a capability did not exist. However, research toward this end was begun by three former students at the Air Force Institute of Technology and their work is summarized below.

Joseph Tatman, GE-79D, (Ref. 5) initially proposed the AFIT Multielectrode Array to extract data directly from the

cortex using contemporary semiconductor technology. Each electrode would have the same approximate size and shape of a BCE. Tatman attempted to build such a device. Although ultimately unsuccessful, his work made possible the development of the first bio-implantable semiconductor brain electrode.

Gary Fitzgerald, GE-80D, (Ref. 6) continued the development of the multielectrode array. Working with Tatman (at the Air Force Avionics Laboratory where Tatman had been assigned after graduation from AFIT), Fitzgerald implemented a 4 x 4 multiplexing scheme: a change which aided array development by simplifying the array circuitry. He also made and tested such an array in air, but unfortunately, tests in saline solution similar to that found in the brain failed because no contemporary encapsulation techniques were capable of sealing the switching circuitry on the chip against sodium ion contamination.

George German, GE-81D, (Ref. 7) considered Fitzgerald's recommendations and explored other possible solutions to this "passivation" problem (i.e. the problem of protecting the semiconductor devices from a hostile cerebrospinal fluid (CSF) or saline environment while at the same time exposing the actual electrode surfaces to the brain). He evaluated sixteen different combinations of materials and application processes but could recommend only two possibilities: phosphosilicate glass (PSG) and polyimide (Ref. 7:36). He

then designed a drive circuit capable of providing multiplexed drive signals to the array and performed preliminary electrical testing in a simulated CSF environment.

STATEMENT OF THE PROBLEM

The primary emphasis of this diverse research concentrates on implanting an encapsulated AFIT semiconductor multielectrode array on the visual cortex of a test animal and collecting sufficient data with which to verify proper operation of the implanted array. Data analysis should reveal the form of the bioelectric signals present. Research into the disciplines required for this extended effort range from semiconductor techniques and integrated circuit design to developing surgical procedures and data analysis with pattern recognition.

The first task involved encapsulating the AFIT array. German recommended two materials, PSG and polyimide (Ref. 7:36), which would have to be evaluated for availability, workability and process compatibility. Environmental interface and packaging problems also needed to be resolved.

In addition, German recommended a redesign of the multielectrode array to improve the Junction Field Effect Transistor's (JFET's) switching characteristics and reduce chip size. He also recommended possible procurement of a commercially-produced version of the AFIT array (Ref. 7:60-61).

It was decided, however, to continue working with

available multielectrode arrays built by Fitzgerald and Tatman since they were at least potentially operable. The external drive circuitry was redesigned from that developed by German taking into account the non-uniform JFET characteristics noted by German (Ref. 7:66-81). The drive circuit had to be simplified and power consumption reduced. Additional circuitry was also required. For example, the previous external drive systems could not operate without actually being connected to a multielectrode array. These chips, however, must be maintained in a protective nitrogen environment because removal from such protection causes contamination degeneration of the operating characteristics. Since there was a very limited supply of chips, it was necessary to design a new drive circuit which would enable the complete drive system (including data recording equipment) to be tested without sacrificing any of the existing multielectrode arrays.

A totally different part of the problem involved the development of surgical procedures for implanting and removing an encapsulated array. Based on a physiological study of the test subject (e.g. baboon, monkey or dog), the exact location of primary visual cortex had to be determined and a simple non-destructive surgical procedure for chronic implant developed.

Finally, methods of data collection and analysis were required. Analysis may require digital programs for digitizing data, presenting visual displays of data, and using complex analytical methods to compute average

transients and relative spatial-temporal activities.

SCOPE

When this research began, the existing stock of 4 x 4 arrays remaining from the work of Fitzgerald and German numbered some 27 units. Some of these had defects which could be discerned by visual inspection and thus, were not useful.

A survey of semiconductor facilities at Wright-Patterson AFB indicated that PSG processing facilities and expertise were not available for this study; whereas polyimide facilities, expertise, and the material itself were available. Consequently, polyimide became the encapsulant of choice.

Although originally designed for implant in a primate, this first implant could be performed on any mammal with an accessible visual cortex of similar size. A laboratory beagle, "Ricky", was available and therefore the surgical procedure was designed for a dog.

An additional limitation was imposed upon data analysis. Data would be collected until the chip failed, the dog expired or three weeks elapsed. However, analysis of the data would be limited to that which was necessary to verify proper operation of the chip and possibly determine the form of collected data. The type of analysis required is complex and time-consuming. It is believed that complete analysis of the data collected from the first implant may require as much as one man-year of work.

APPROACH AND PRESENTATION

This research is presented in essentially chronological order. Each chapter represents a different phase of this research and contains an approach to the problems incurred and their resolution.

Chapter II presents a discussion of the AFIT multielectrode array and its development into an implantable probe. Topics discussed include initial assumptions, the encapsulating process and packaging problems.

Redesign of the external drive circuitry is presented in Chapter III, with justification and diagrams. The printed circuit board and chassis are shown in diagramatic and pictorial form.

Chapter IV discusses how the individual devices were integrated into an experimental system and thoroughly tested. There is a discussion of comprehensive system testing without the array, followed by a discussion of array and system testing in a simulated CSF environment.

Chapter V addresses preparations required for the implant and the surgical procedures developed.

Chapter VI details data collection and the Visual Evoked Response (VER) method. Discussions pertain to data about the array itself, the data collected and physiological data about the test subject.

Chapter VII draws conclusions about the array, implant, hardware and data. In particular, conclusions are drawn about this method of data collection and its validity.

Chapter VIII presents recommendations. There are recommendations about the array, hardware, external drive circuitry, surgical and test procedures, and data analysis.

Equally important is the information contained in Appendix F. In parallel with the major portion of this fifteen-month research effort there was an additional endeavor to obtain a commercially-produced version of the AFIT multielectrode array. Another parallel effort successfully integrated the multiplexing circuitry with the multielectrode array on the same substrate. Together, these comprise a major portion of the redesign required for a "second-generation" multielectrode array.

CHAPTER II

DEVELOPMENT OF AFIT ARRAY AS A SURGICAL IMPLANT

BACKGROUND

As mentioned in the introduction, this is a continuation of other research efforts, the most recent being a study of protective or encapsulating materials by German (Ref. 7). Having laid the ground work, German provided a suitable beginning point for the study. As a result of his research, two encapsulating materials emerged as "the most promising", polyimide (PI) and phosphosilicate glass (PSG). Of the two candidates, polyimide was selected for further encapsulation testing, because of its ease of processing and the availability of needed processing facilities and equipment. Furthermore, in conversations with German, he recommended polyimide more highly than PSG (Ref. 8).

In most industrial cases, PI is used as a passivating layer between two metal layers on a microcircuit (Ref. 9, 10). However, the interest here is to "passivate" the array from cerebrospinal fluid (CSF); the method employed is to use polyimide as an encapsulant over the array as opposed to a passivation between any layers of the microcircuit itself. A major concern, as will be detailed later in this chapter was the etchability of polyimide. Although polyimide films may be masked and etched, the etchability problem had not been considered relative to the particular processing problems involved with AFIT arrays.

However, etchabilty was assumed and polyimide was used. The real issue then, was to determine the best etchant and etch rate for the encapsulation processing.

ENCAPSULATION

The most pressing issue at this point in the study was the reliability of polyimide as a long term encapsulant as well as the validity of the preliminary tests accomplished with PI. It is important to note that the objective at the outset was to prove a polyimide encapsulation had an operating life of "several hours". The subjective feeling was that even a few hours of reliable operation warranted the time, effort and energy involved in actually performing an implant and collecting data. With this objective in mind, testing began.

The first test was an attempt to reproduce German's results (Ref. 7:57-58). After examining German's procedure and the manufacturer's polyimide processing recommendations (Ref. 7, 11, 12, 13), three modifications were made in an effort to obtain better results (i.e. higher probability of survival in a saline environment). The procedural changes are as follows:

1) "Puddle" polyimide into the mounting header "well" (Figure 2-1) instead of using a spin application method.

2) Substitute PI 2555 for PI 2545.

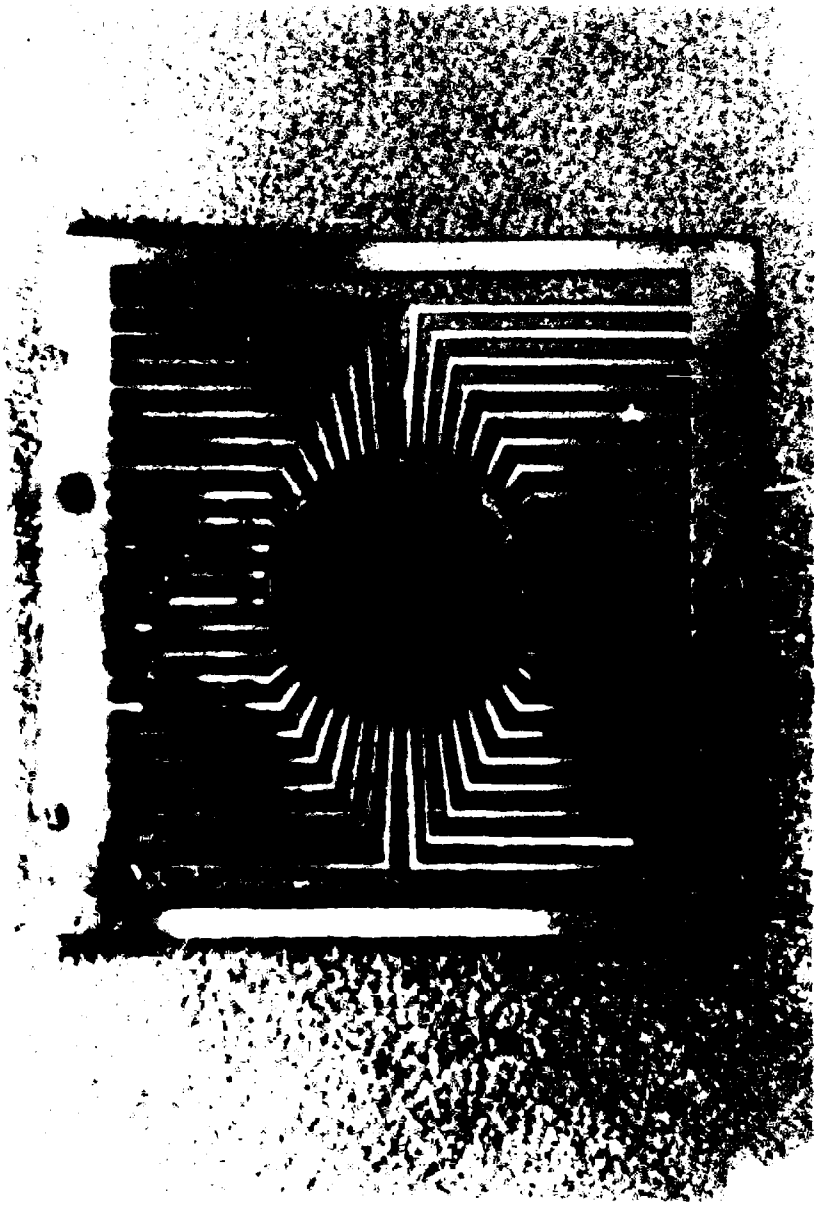
3) Modify the cure sequence to accommodate PI 2555. (Pre-cure thirty minutes at 120 degrees centigrade; then complete the cure at 180 degrees centigrade for two hours.)

Technically, if the procedure German used was thought questionable, that procedure would have been followed exactly to verify his results. However, reproduction of similar results was highly probable and changes were introduced only to improve on the results of the previous experiments.

After stepping through the modified procedure and following the final cure and cooling period the integrity of the encapsulation was examined. Although the manufacturer's processing recommendations are for films on the order of one to two microns (Ref. 12), this preliminary experiment filled a one millimeter deep depression with non-dilute PI. The manufacturer's recommended curing procedure was also used and even though this was a "thick layer", the polyimide appeared completely cured. Similar to German's procedure (Ref.7:57), the 4 X 4 array of 0.001 inch diameter wires which were bonded to the sixteen JFET source pads, were exposed by "shaving" off a thin layer of the cured polyimide. Figure 2-1 shows the mounting header and the cured polyimide filling the header well. The raised areas in the well are loops introduced by the bonding wires as they transition from one point of attachment to the next.

FIGURE 2-1

ENCAPSULATED ARRAY IN MOUNTING HEADER



The encapsulated array was placed in a "needle-probe" assembly and each JFET was tested. This check was simply to identify which JFET's on the array were functional and was not intended to verify the operation of the array, which as discussed later, had not been proven.

As documented in German's research, the characteristics of any JFET on an array may not be identical to any other JFET on the same array. In fact, there was no guarantee the encapsulated array had any functional JFET's. The first test then, was to identify those functional JFET's on the now encapsulated array. Using a needle-probe assembly and microscope, a signal of known frequency and amplitude was injected into each JFET source individually via the wire bonded to it. At the same time, the appropriate JFET gate was pulsed using the drive circuit (Chapter 3) and the corresponding drain was examined as the output. By this method, the functional JFET's were identified. It turned out that all the JFET's on this array were functional with no apparent cross-coupling between any two. Although functional, three of the JFET's could not be completely "pinched off". Also, as expected, though of little consequence to us at the present time, each JFET exhibited different operating characteristics. Now having verified the JFET's on the array individually, the next step in our preliminary verification of polyimide as an encapsulant was to make all the necessary connections from the array to the drive circuit.

In addition to the bonding wires attached to the electrode pads, point-to-point connections had also been made from each of the four rows and columns on the array to separate header pins. A wire was soldered to each of the appropriate header pins thus providing a semi-permanent means of connecting the AFIT array to the drive circuit. Finally, the encapsulated array had to be subjected to a simulated environment while operating. To facilitate this portion of the test, the header was attached to a short steel rod with epoxy glue. Also, the header, all solder points, and everything up to the header well was protected with epoxy. This was necessary because the entire header would otherwise come in contact with a saline solution causing an electrical short circuit and destroying the array. After the epoxy had been applied and dried, only the ends of the sixteen wires in the polyimide coating were exposed. This preparation was far from implantable but served to give an indication of the life expectancy of the PI encapsulant.

To begin testing, a signal was induced across a simulated "test brain" which consisted of a pad of paper towels moistened with physiological saline solution (i.e. sodium chloride, 0.9% in water), and the array was connected to the drive circuit. The array was lowered onto the moist surface and immediately the signal on the "brain" was sensed by the AFIT array and accompanying drive circuitry. Because of non-uniform JFET characteristics the output signals contained a DC offset. Most, but not all, of the biases

were adjusted out of the signal using the compensation mechanism built into the drive circuit (see Chapter 3). It was noted that the JFET characteristics were neither identical nor ideal; however, the purpose of this test was to prove the polyimide encapsulant and not the array fabrication.

Had there been any major defects in the PI encapsulation or in the epoxy protecting the header pins and solder points, the device would have failed almost immediately as earlier units had when immersed in saline solution (Ref. 6:84). However, after one hour of continuous operation, the array was still functioning properly. After twenty-four hours, the array was removed from the saline solution and the PI layer was examined. There were no detectable surface deformations or defects as a result of the test thus far. A decision was made to continue testing the array in the saline solution until there was noticeable degradation in its operational capability. After forty-eight hours, the JFET characteristics had shifted. The DC offsets were again balanced to compensate for these shifts. (The shifts are due to an electrode quieting period (Ref. 14:201-203). By sixty hours of operation the array was clearly failing. Under microscopic examination, some water absorption in the polyimide coating was found; most likely a result of insufficient curing. It was not visually evident that the saline solution had permeated to the array surface itself but array failure suggested that it had.

With this success, efforts turned to developing an application and etching technique which would yield similar results.

POLYIMIDE APPLICATION AND ETCHING TECHNIQUES

In the development of an implantable microelectrode array, a procedure must be developed for reliable application, masking and etching of polyimide films. The development of such a procedure will permit fabrication of a probe small enough to be used as an implant. The manufacturer's processing recommendations were used as a bench mark (Ref. 11, 12, 13, 15, 16).

In all testing, a spin application method was used. Although film thickness varies with spin rate and solution concentration, no effort was made to correlate these factors. The objective was only to find a spin rate and concentration which provided a "good" PI layer (i.e. a uniform layer several microns thick). The results of this testing are presented below. Appendix C presents the final processing schedule used in processing the microelectrode array which was implanted.

Four polyimide concentrations were tested in an effort to find a concentration which 1) after final cure, provided a uniform, essentially non-defective layer, 2) yielded the "best" etch characteristics and, 3) sufficientlv encapsulated the array. All tests were conducted using clean (see Appendix B, schedule 1) non-patterned silicon wafers, some with and some without silicon dioxide (SiO_2)

layers. Wafers processed without using an adhesion promoter or without a layer of silicon dioxide were unsatisfactory. In both cases, the polyimide film pulled back to the center of the wafer in a bead. This indicated that either an adhesion promoter (Ref. 17) or an SiO_2 layer had to precede the PI coating.

Once the adhesion problem was overcome, testing of the different solution concentrations began. Efforts to conduct pinhole/defect analysis of the cured PI films were not made. Rather, a subjective rating system was used to determine the "best" PI/thinner ratio with regard to the three criteria above. Equipment availability and time were limiting factors in this area. Since film defects had been studied (Ref. 7), a subjective score was believed sufficient for comparison. The rating scheme involved four factors for each PI concentration and each etchant used. They are:

1) Quality of film, or film integrity, after final cure without etch.

2) Film integrity after final cure having etched a pattern in the film.

3) Etchability; referring to the ease of etching the PI layer (including consideration for variations in temperature and cure time).

4) Integrity of the etched pattern.

Each factor was rated on a one-to-ten scale and is explained below respectively.

1)	1-major film defects; cracks, holes apparent nonuniformity	- to -	10-uniform, defect free polyimide layers
2)	1-major film defects; cracks, holes poor pattern definition	- to -	10-uniform, defect free layers, well defined patterns
3)	1-etch difficult to control, timing too critical, incomplete etch, poor pattern definition	- to -	10-reliably predictable etch rate well defined patterns
4)	1-severe undercutting all or part of wafer unetched, poor pattern definition	- to -	10-good pattern definition no apparent undercutting

Tables 1, 2, and 3 show the subjective score for each factor at each PI:thinner ratio for the three different etchants tested.

Plasma etching was the first etching technique examined. Table 1 presents the scores for each category using plasma (i.e. O_2) as the etchant. Repeated trials at every PI concentration yielded poor results due to equipment difficulties. A plasma etch is a practical method of etching partially cured PI films; however, the plasma "asher" (i.e. low temperature RF plasma asher) available for this study did not etch uniformly over the entire surface of the wafer. Therefore, because no other asher was available, other etchants were investigated. Nonetheless, though one side of the wafer would be more etched than the opposite side for any given etch, a score was assigned based

on the worst area on the wafer. The low ratings for etchability and pattern integrity with full strength PI are probably a result of trying to etch a thicker film. Further investigation was not pursued, but a faster spin rate, a longer spin time or both would yield a thinner film, even with full strength PI and thus better etching characteristics.

Table 2-1
Polyimide Film Quality: Subjective Rating
(Plasma Etch)

PI/ Thinner	Film Integrity	Integrity after etch	Etch-ability	Integrity of pattern
1:0	8	6	3	4
2:1	5	5	7	6
4:1	7	6	7	6
5:1	8	8	7	6

The next etchant examined was an alkaline solution. Manufacturer's recommendations included a suggested alkaline etchant of potassium hydroxide (KOH) in deionized water (DI) (25 grams KOH in 500 milliliters DI water). Wafers were etched by dipping the entire wafer into the etch solution. The alkaline etchant proved extremely unreliable.

The etch time was highly variable, taking from thirty to ninety seconds. This variability was due to solution age, and the number of times used. In an effort to reduce

the etch time variability, a new solution was prepared for each day or each time a solution had been used to etch ten wafers. By keeping the solution fresh, the variability of the etch time was reduced. The nominal etch period was thirty seconds with a three to five second variation. Nonetheless, timing was still a critical factor. At best, one had to make an educated guess of when to remove the wafer from the etchant. Slight variations in film thickness, cure temperature and or cure time, mandate slight variations in the etch time. The problem is, however, that none of these variations can be known exactly before the etch, thus, corresponding variations in the etch time cannot be predetermined. Unfortunately, the quality of etch is dependent upon knowing the correct moment to remove the wafer and stop the etch. Table 2 shows the subjective scores based on the results of the testing. The results were unsatisfactory and the alkaline etch was abandoned.

Table 2-2
Polyimide Film Quality: Subjective Rating
(Alkaline Etch)

PI/ Thinner	Film Integrity	Integrity after etch	Etch-ability	Integrity of pattern
1:0	8	3	2	1
2:1	5	2	1	1
4:1	7	3	4	3
5:1	8	3	4	3

Although other etchants are available, the final etchant tested was positive photoresist developer, AZ351. The search for an etchant stopped here primarily because this etchant was reliable. Though the etch rate was fast, it was predictable. The AZ351, diluted 1:5 with DI water (1 part AZ351 to 5 part DI water) and a spin-spray method were used for etching.

The tested PI concentrations etched at different rates. The 2:1 concentration was the most difficult to etch reliably because the etch rate was too fast. With the standard cure time and temperature, the 2:1 concentration could not be etched slowly enough to prevent significant pattern deformation. Increasing the cure time yielded a predictable etch rate, but the resulting pattern definition was poor. (An alternative not pursued would be to reduce the etchant concentration.) Similarly, though the full strength PI etch rate was predictable, the thickness of the layer prevented etching completely to the wafer surface without significant undercutting. Once again, alternatives were not investigated.

The 4:1 and 5:1 PI concentrations exhibited very similar film integrity and etch characteristics. The 5:1 ratio was slightly better in both categories. The superiority of the 5:1 solution and the positive photoresist developer etchant precluded testing other PI concentrations. Though Table 3 is based on initial tests, further testing yielded the same qualitative ratings for the 5:1 solution.

At this point, further tests were conducted with the 5:1 PI to establish the best values for cure time before etch, and cure temperature.

Table 2-3
Polyimide Film Quality: Subjective Rating
(Positive Photoresist Developer Etch)

PI/ Thinner	Film Integrity	Integrity after etch	Etch-ability	Integrity of pattern
1:0	8	8	7	5
2:1	5	5	4	5
4:1	7	7	7	8
5:1	8	8	9	8

The first of these parameters must be approached with two considerations in mind; First, cure time at a given temperature and second overall cure time. (Realistically, the cure time should not vary more than a minute or two. However, a range which would yield acceptable etch characteristics would allow for inadvertant processing delays.)

Wafers were processed according to the schedule in Appendix C with variations in cure time introduced as follows. First, ten minutes was added to the partial cure time, then the partial cure time was reduced by ten minutes. The second parameter, cure temperature for the partial cure, was varied by five degrees centigrade while using the

nominal cure time with the above variations. Having tested all variations of cure time and cure temperature as above, no noticeable degradation appeared in the PI layer or the etched pattern.

The motivation for this range determination stems from the unreliability of the equipment used for processing. An uncalibrated convection oven was used for all curing. Achieving the same temperature from day to day was impossible but not extremely critical. Variations ranged from plus-to-minus five degrees centigrade. Additionally, though all process steps were timed, there were variations in operator response time. Thus, though nominals exist, they cannot always be precisely achieved. As pointed out above, it turned out that it did not matter.

PACKAGING

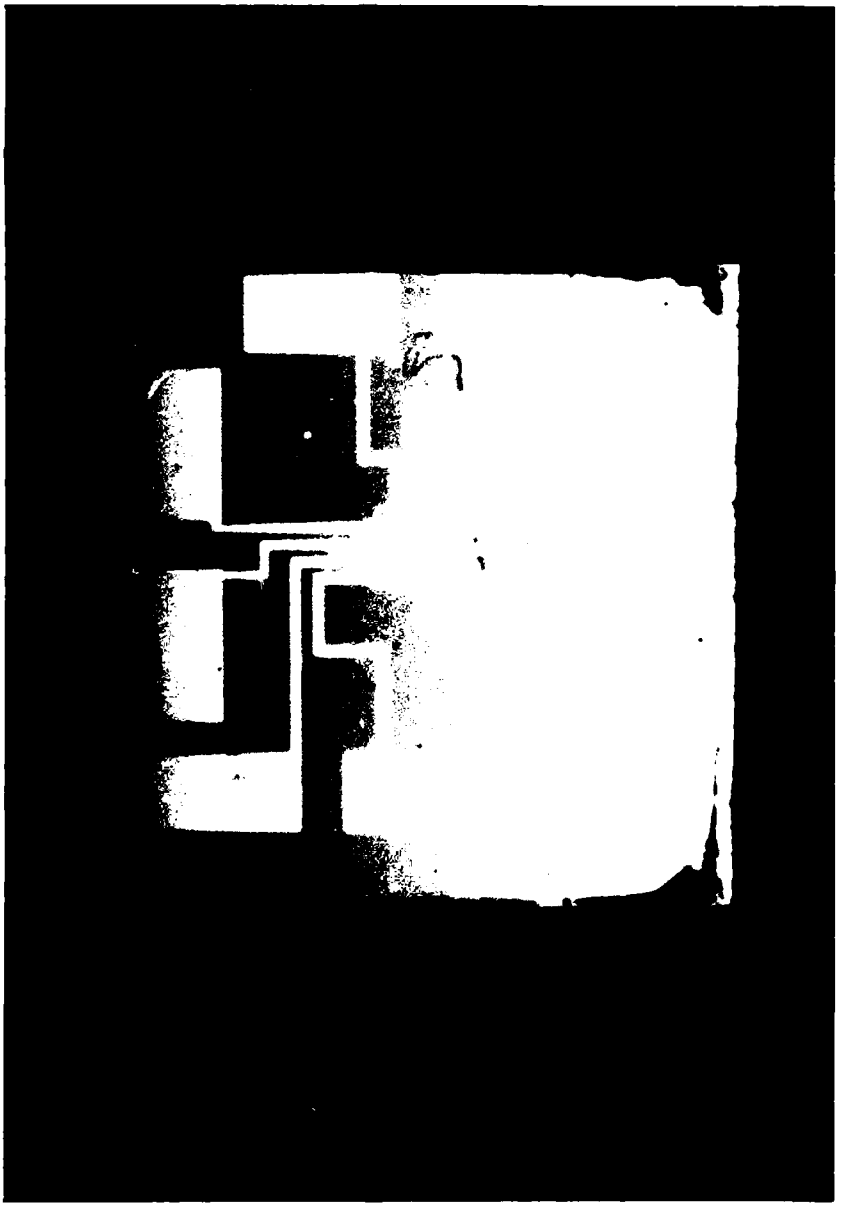
Packaging became a major consideration in this very nonstandard semiconductor process. Two things are important. First and foremost is the finished product size, and second is the electrical interface required to connect the microscopic world to the macroscopic world.

Implant Considerations

Size and shape constraints are significant considerations because this device is to be implanted on the primary visual cortex of a laboratory animal without a craniotomy. Thus, it is paramount that total package thickness be kept to an absolute minimum. Package shape is

FIGURE 2-2

APIT ARRAY WITH BONDING PADS



also a consideration because the device must contact the cortex without causing significant deformation of the cortical surface.

The area of silicon on which the AFIT array is fabricated is a one centimeter square. As Figure 2-2 shows, this includes the array and bonding pads. The minimum package size then is a one centimeter square. However, wires bonded to the array side of the silicon chip must be bent around the edges and bundled on the backside of the chip. Therefore, the length, width, and thickness of the final product must necessarily be somewhat larger than a one centimeter square. Preparation of the actual device which was implanted in the dog's skull is described below. Chapter VIII recommends some changes to this packaging preparation which will reduce the size of an implanted array-package (probe) assembly.

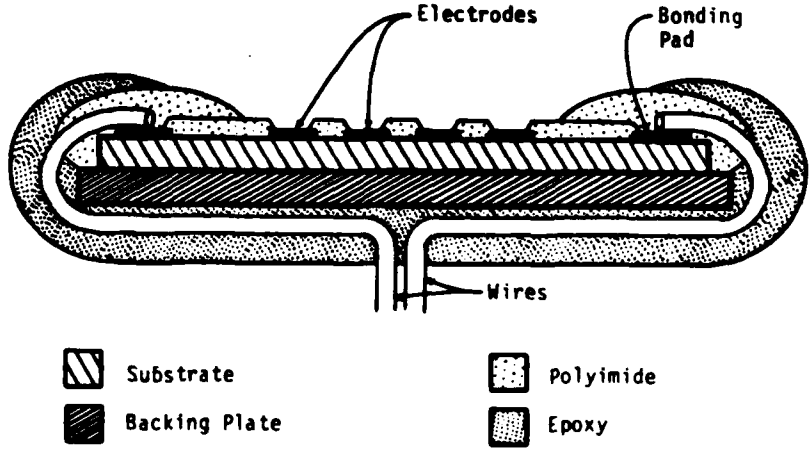


FIGURE 2-3

SIDE VIEW OF FINAL PROBE PREPARATION

Figure 2-3 is a side view representation of the implanted probe. After encapsulation, electrical interface and structural integrity dictated package size and shape. It was necessary to enhance the strength of the array to reduce the possibility of breakage during handling. To do this a one centimeter square piece of silicon from a test wafer was cut and attached to the back of the AFIT array using polyimide as an adhesive. Next, nine small diameter wires (35 AWG) were attached to the array bonding pads using silver contact paint. Once the connecting wires were securely in place they too, had to be encapsulated since the entire probe would be in a saline environment after implant. This encapsulation was accomplished by dabbing PI over the wires at the contact points and outward toward the array as close as possible without risking spill-over into the already open contact windows. This PI "layer" was cured via the procedure outlined in Appendix B. For additional encapsulation and structural integrity, epoxy (Extra Fast Setting EPOXY, Cole Parmer Instrument CO. Chicago, ILL.; order number 8778) was dabbed over a part of the polyimide just cured, around the edges of the chip and over the entire back-plate surface. This preparation yielded an encapsulated probe which would withstand handling and implant. The resulting "package" was however, large relative to the animal's skull and brain. Nonetheless, this was the best device available at the time. Therefore, it became the implant.

Electrical Interface

The second problem, that of connecting the array to the outside world has been mentioned. However, the reason for this problem arises from nonstandard processing. Typically, a microcircuit is packaged in a header of one sort or another (i.e. DIP, flat pack, etc). The interface to the outside world is accomplished by ultrasonically bonding small diameter wire (on the order of 0.001 inch) to appropriate points on the microcircuit and then to appropriate pins on the header. The package is then hermetically sealed. Thus, protecting the fragile piece of silicon structurally and electrically.

Most package headers are not large enough to accommodate a piece of silicon one centimeter square and those which can, were much too large to serve as an implant. Therefore, as previously noted, an alternate means of packaging was required. Additionally, as described in chapter III, a Molex connector was attached to the signal wires so the device could be tested under simulated operational conditions. Although each wire was insulated by a lacquer coating, the bundle of wires from the back of the chip to the Molex connector was protected in a nontoxic, surgical elastic tube.

This potentially implantable preparation now had to be tested. Chapter IV discusses such testing and support equipment. However, prior to array testing a suitable drive circuit external to the array itself, had to be developed.

CHAPTER III

EXTERNAL DRIVE CIRCUITRY

AFIT MULTIELECTRODE ARRAY

The AFIT multielectrode array is a four-by-four array of Junction Field Effect Transistors (JFET's) as shown in Figure 3-1. In this electrical diagram of the AFIT array, each source is shown connected to a square "sensing pad" through which signals present on visual cortex are conducted. All gates of each "row" are connected as are all drains of each "column". A reference electrode (REF) is also provided.

When multiplexed signals (Figure 3-2) are applied to the rows, information present on the sources of a particular row are passed through the JFET drains to the column outputs. Thus, sequential selection of the rows produces a multiplexed output at each column. Figure 3-3 shows the basic format of the column output. Notice that information is present only on column n when row n is enabled (i.e. n= 1,2,3, 4) because the information signals were applied to only row n column n sources. If information was applied to all 16 sources, a diagram similar to Figure 3-3 would show a four channel multiplexed output with information present on all four columns. A combination of several signal generators was used to produce the "information".

The design and JFET technology of the AFIT multi-electrode array impose numerous constraints upon the

Figure 3 - 1

AFIT Multielectrode Array

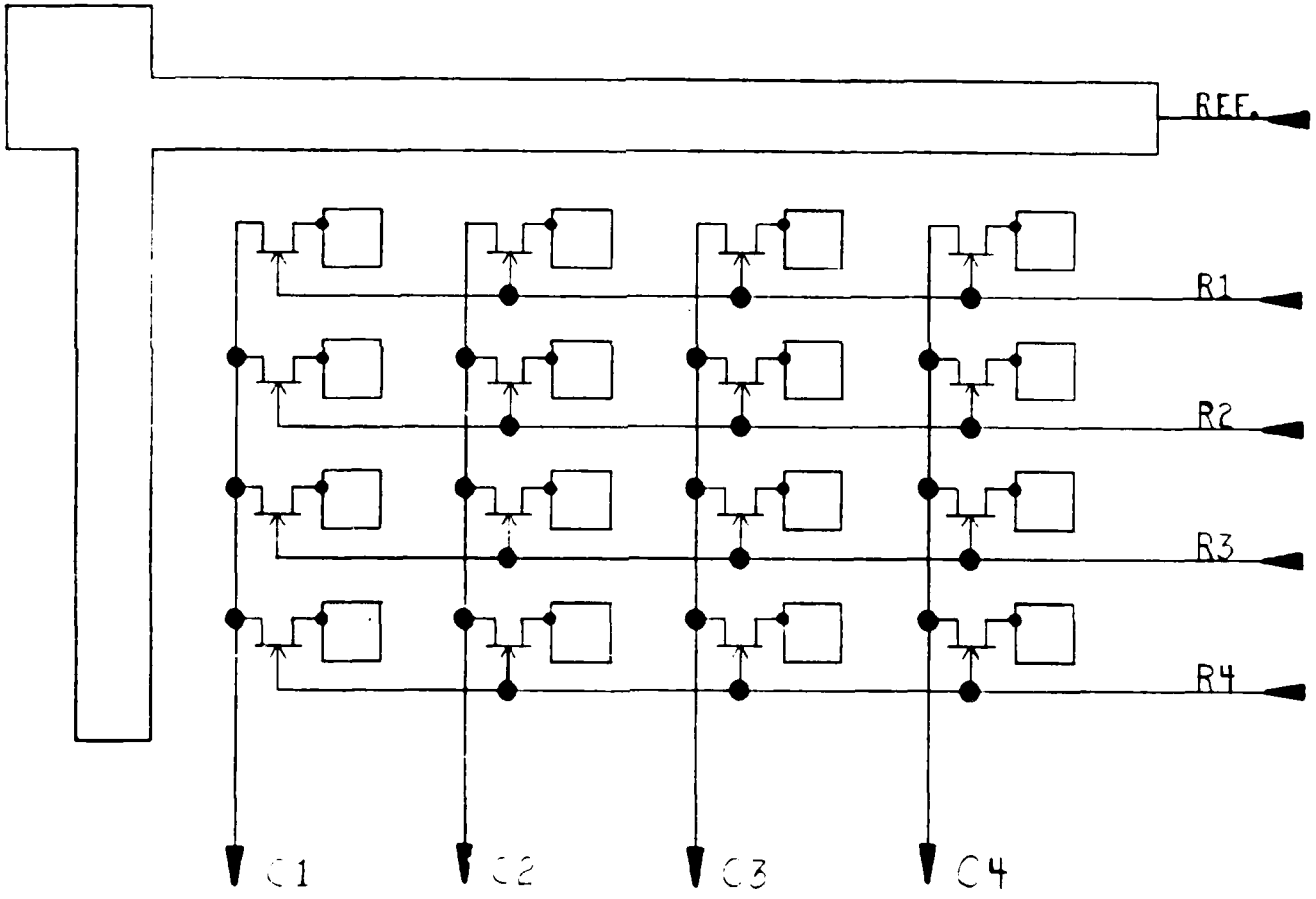


Figure 3-2 Row Input

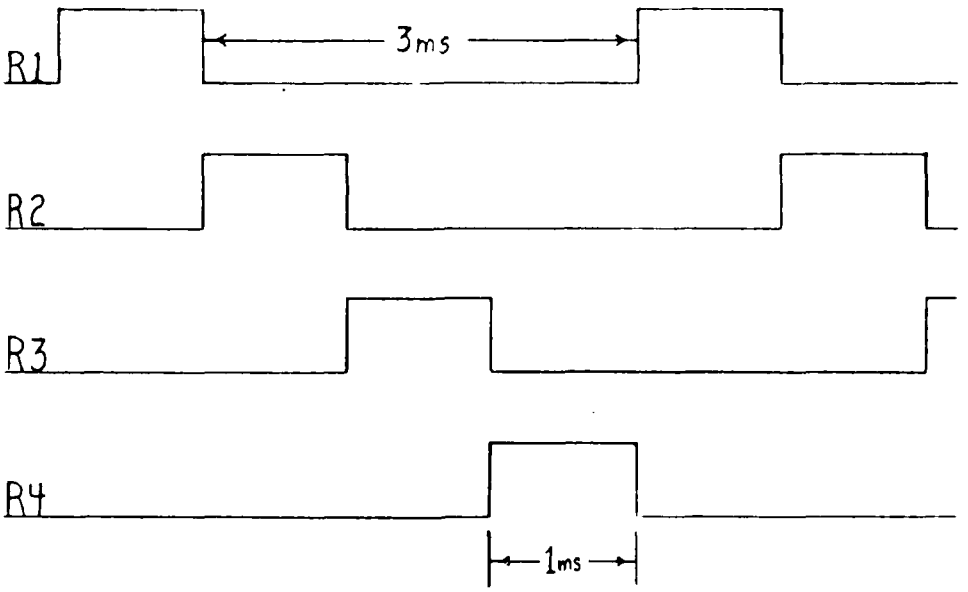
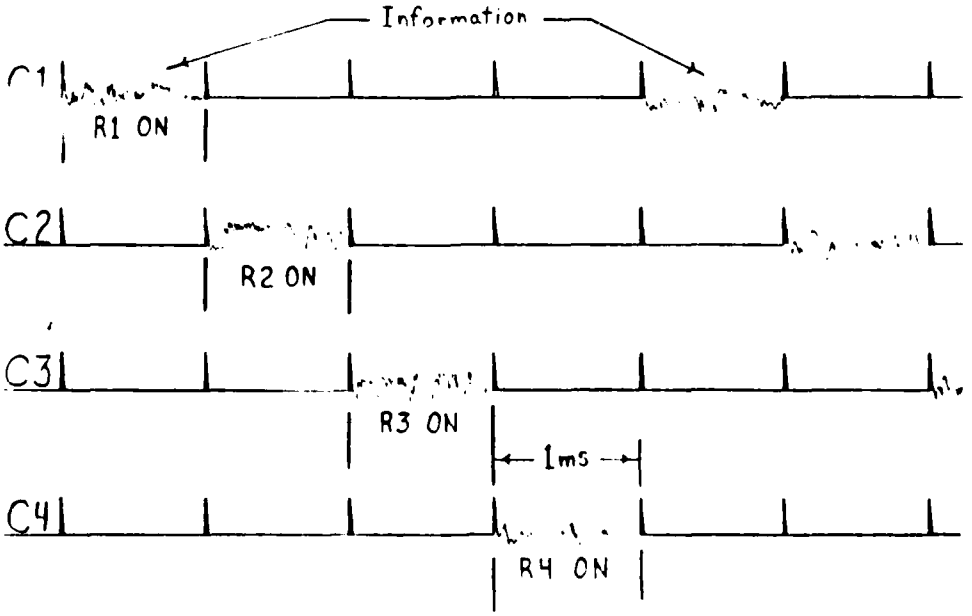


Figure 3-3 Column Output



external (i.e. external to the AFIT array integrated circuit shown in Figure 2-2) circuitry required to provide the row inputs and amplify the 20 to 50 microvolt signals present on the column outputs (Ref. 18:365-366). Row inputs must be multiplexed and voltage compatible. That is, the input cannot exceed the maximum gate voltage and must be at least one volt less than the "pinch-off" voltage (Vp) to provide switching action. The external drive circuit must be capable of providing these signals for multiple AFIT arrays.

Column output signals are much smaller than the 60 Hertz (Hz) electrical noise produced in most power supplies. In fact, 60 Hz noise due to fluorescent lighting and other electrical devices is often greater than 50 to 100 microvolts. The use of batteries eliminates the 60 Hz noise produced by a power supply; and shielding of the external drive circuitry and signal wires significantly reduces the effects of 60 Hz noise in a room.

Although the external drive circuitry designed by Captain German (Ref. 7:40) meets the noise-related requirements and is capable of driving a single AFIT multi-electrode array, any additional arrays would require additional drive circuits.

REDESIGN CONSIDERATIONS

The decision to redesign the prototype external drive circuitry used by German was based on several factors. First, the size of German's external circuitry was too large. Each drive circuit required six integrated circuit

packages with associated resistor and capacitor networks. Second, the power requirements of the drive circuit necessitated the use of relatively large batteries. Third, if it were possible to reduce the supply voltage, fewer batteries would be required and total power consumption would be reduced. Fourth, intervening experimentation revealed the need for additional functions. Fifth, a back-up drive circuit was needed in case the first drive circuit failed.

REDESIGN

Device Selection

Complementary Metal-Oxide Semiconductors (CMOS) devices were chosen for six basic reasons:

1) Low power dissipation (Less than 10 mW per gate)
2) Short Propagation delays (25 nanoseconds/gate)
3) Good noise immunity
4) Operation over a wide range of supply voltage
5) Elimination of need for Field Effect Transistor (FET) switches (MC14016)
6) The availability of Large Scale Integrated (LSI) devices

Therefore, subsequent redesign used only CMOS devices.

Power Reduction

Research into the CMOS family of integrated circuits led to a rather simple drive circuit which considerably reduced power consumption. An MC14538B (Appendix D) dual monostable multivibrator is used as an oscillator. An

MC14022B (Appendix D) Johnson Counter decodes the oscillator pulses into one of four outputs. These two LSI circuits perform all the functions of the external drive circuit while considerably reducing size and power consumption. Power consumption is further reduced by operating these chips at 6 Volts instead of 12 Volts.

Frequency Selection

There is evidence (Ref 19:26) that 25 Hz is the highest frequency of any signal present on the visual cortex. In multiplexed circuits, a sample rate ten times the highest frequency assures a quality reproduction of the original signal. Thus, each of the four column outputs must be multiplexed at 250 Hz. There are four multiplexed outputs, therefore, the oscillator frequency must be 4 x 250 Hz, or 1 kilohertz (KHz).

Multiple Arrays

Each output of an MC14022B counter can provide up to one milliamp of current. Thus, a single output could theoretically drive 50 to 100 multielectrode arrays in parallel. For example, Row 1 of all the n, (where n is any number between 1 and 100), multielectrode arrays could connect in parallel to any output of the MC14022B. This parallel capability eliminates the need for additional circuits which were previously required for the synchronization of the n multielectrode arrays. However, CMOS fanout is more severely limited by capacitive loading

than by current loading. Therefore, fanout to n multi-electrode arrays is dependent upon the total capacitive load of the n parallel multielectrode arrays and connecting wires. Empirical evidence suggests a realistic fanout of twenty multielectrode arrays but validation is impossible since less than twenty currently exist.

JFET Characteristics

Each of the multielectrode's sixteen JFET's should ideally possess the same operating characteristics. At present, however, such is not the case. In fact, the JFET's on existing multielectrode arrays may each have a different pinch-off voltage, "off-resistance" (R-off) and "on-resistance" (R-on) (Ref 7:18).

One method of compensating for the "off-resistance" is shown in Figure 3-4. Each MC14022B output signal is applied to a variable resistor. The resistor output is used to control the pinch-off voltage applied to a row of JFET gates. This compensates for "off-resistance" of JFET's in one row with respect to another. Although the ability to compensate for each discrete JFET is desirable, the present design with a 4 x 4 multiplexed array prohibits independent compensation.

"On-resistance" differences are compensated by varying the load resistance (Figure 3-5). The load resistor is in series with R-on and can be adjusted to compensate for any differences which may exist between column outputs.

Figure 3-4 R-Off Compensation

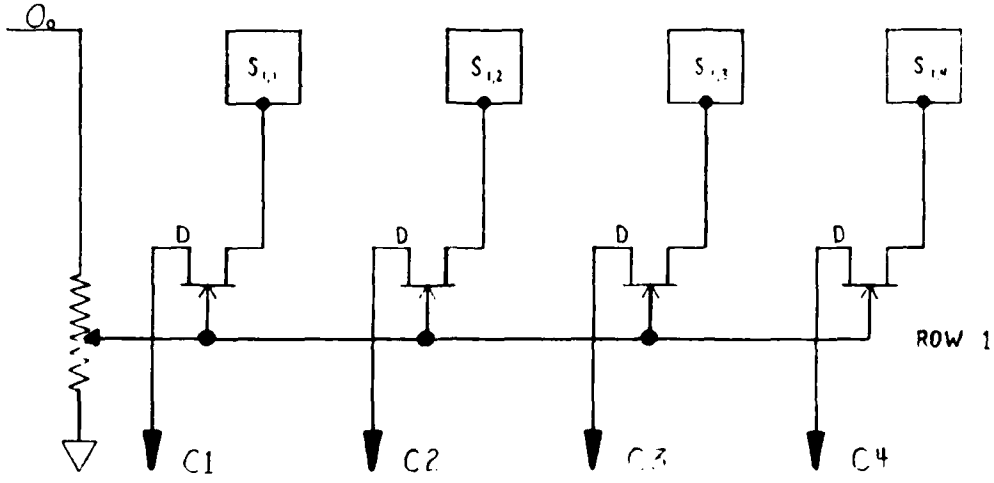
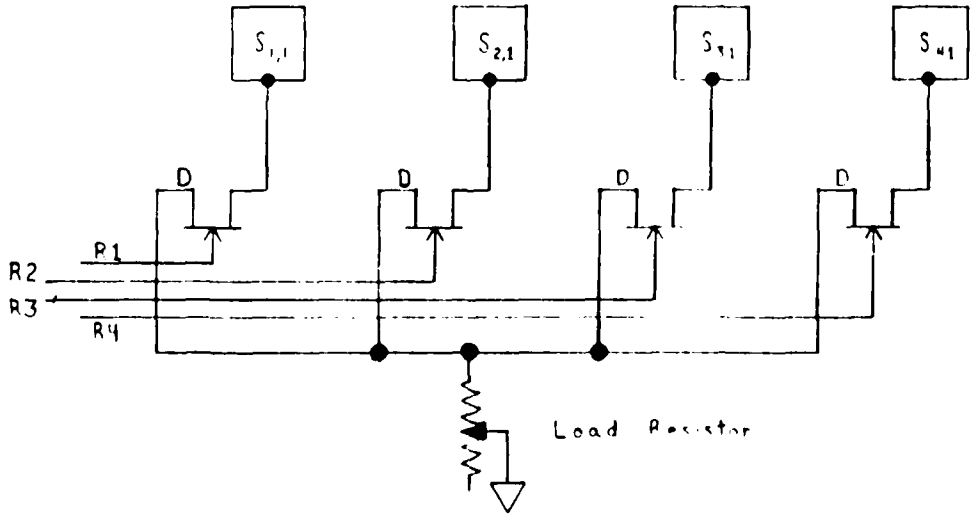


Figure 3-5 R-ON Compensation



Output Measurement

Voltage signals are usually measured with respect to a common (or ground) within a circuit. This is known as absolute voltage measurement. The external drive circuitry, however, must provide a convenient method for differential voltage measurement. The ability to measure output signals differentially permits direct comparison with electro-encephalographic (EEG) data, the form of which is well-defined.

Independent Operation

While the AFIT multielectrode array and its external drive circuitry were developed separately, one cannot function without the other. Hence, without the AFIT array, it is impossible to develop, modify, or test the drive circuitry. This problem is easily overcome by using four JFET's to emulate operation of the AFIT array. With this minor addition, the external drive circuitry can operate completely independent of the array.

VER Requirement

The ability to extract meaningful information from the visual cortex depends upon the visual stimulus provided. One technique, visually evoked response (VER), often uses a strobe light as the stimulus. The strobe light must be accurately timed and synchronized with the data.

A 2 Hz multivibrator which performs these functions was added to the external drive circuitry.

THE EXTERNAL DRIVE CIRCUIT

The Multivibrator

A 1 KHz fundamental frequency is produced by a cross-coupled multivibrator configuration (Figure 3-6). The heart of the multivibrator is a Motorola MC14538B, Dual Retriggerable Resettable Monostable Multivibrator (Ref. 20). For operating specifications and pinout refer to Appendix D. Cross-coupled implies that an output of each multivibrator is an input to the other.

Figure 3-7 shows functional and timing diagrams for the cross-coupled multivibrator. Each multivibrator (one-shot) triggers on the leading edge of the input signal. The Q' (Q complement) output of one is the input to the other (i.e. regenerative feedback). The time constant established by R1 and C1 produces a 300-microsecond inverted pulse at pin 9, the Q' output of one-shot A. When a leading edge occurs at the end of the 300-microsecond pulse, one-shot B fires and produces a 700-microsecond pulse at pin 7, its respective Q' output. Capacitor C2 and resistors R2 and R3 establish a 700-microsecond period. Variable resistor R3 permits fine adjustment of the 700-microsecond period. The total period for one cycle is 1 milisecond, which corresponds to a frequency of 1 KHz. The "clear" function is not used and therefore, is strapped high (VDD) at pins 3 and 13.

Figure 3-6 Multivibrator

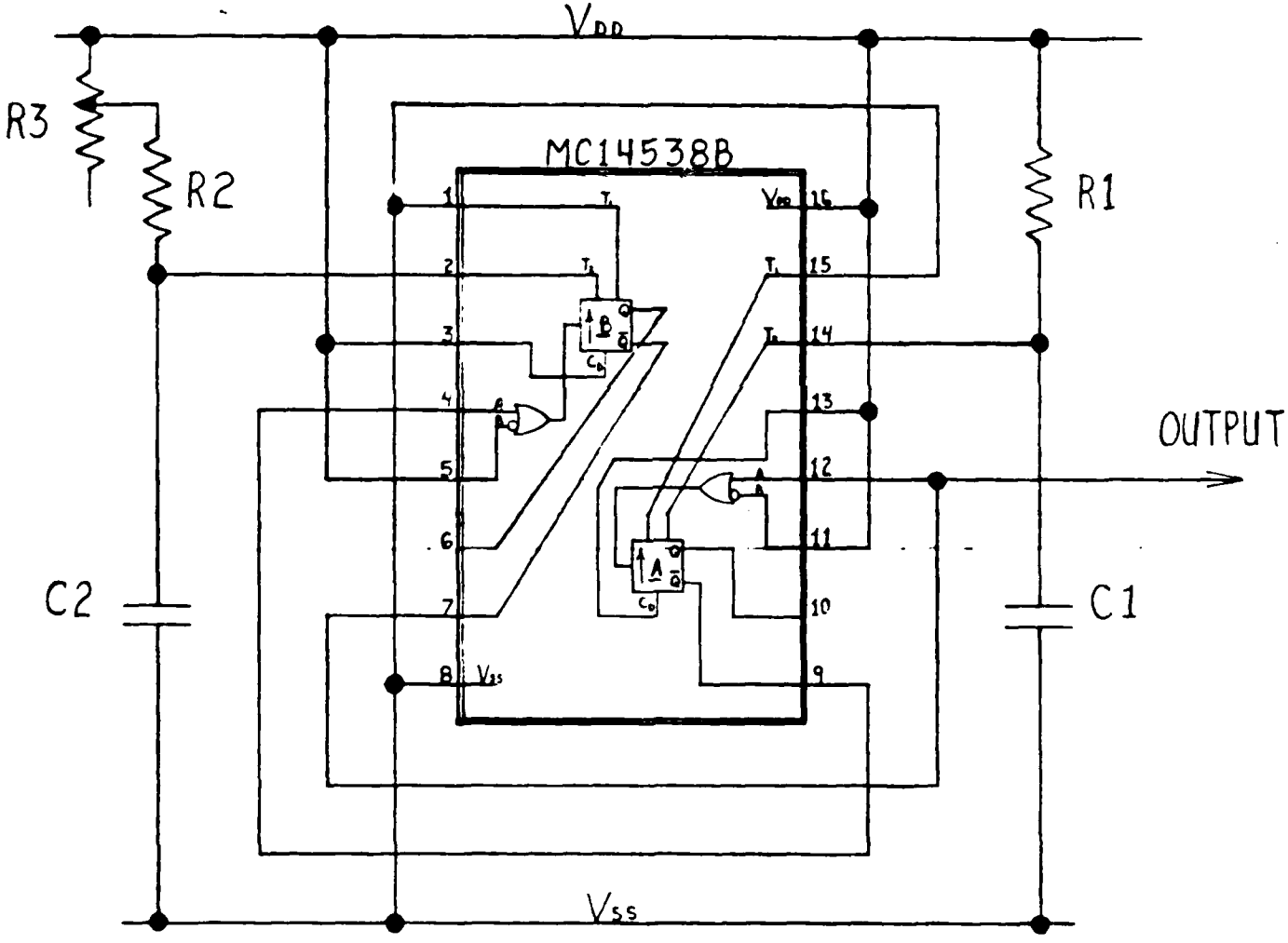
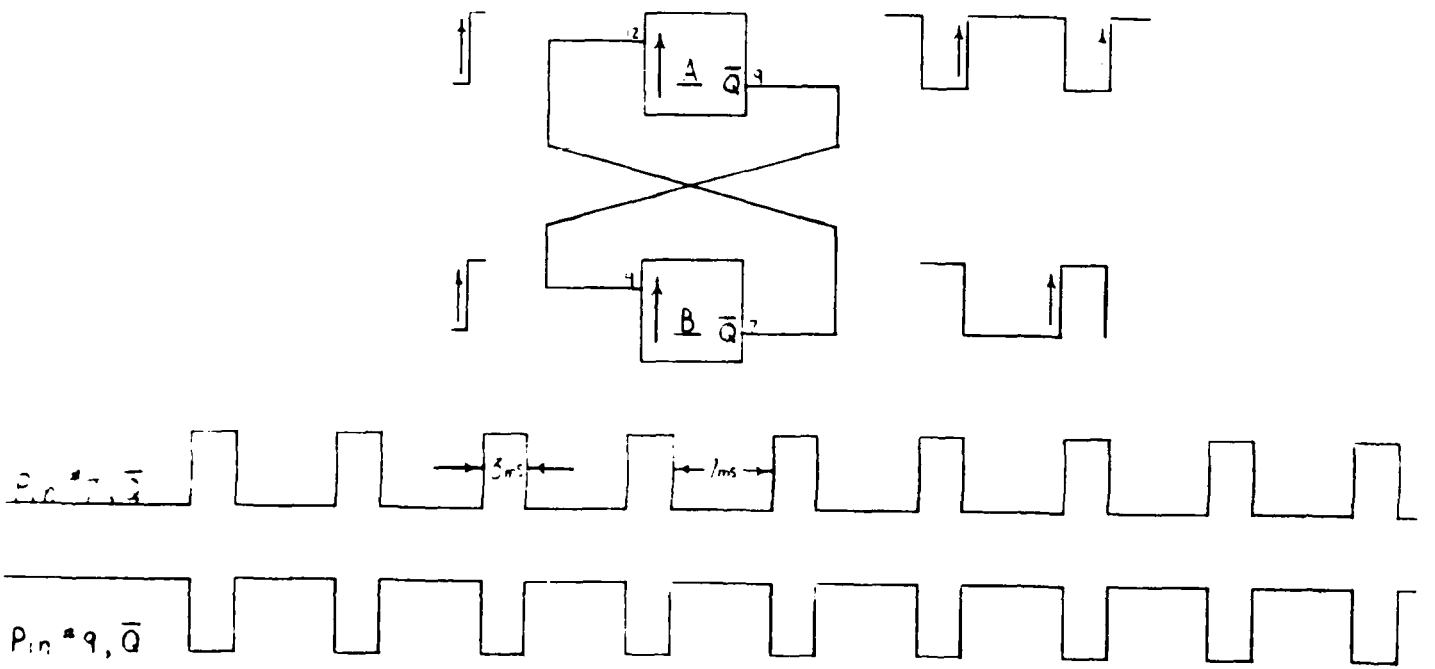


Figure 3-7

Cross-Coupled Multivibrator



A Johnson Counter

A divide-by-four function is executed by a Motorola MC14022B, a 4-Stage Divide-by-8 Johnson Counter (Figure 3-8) (Ref. 20). Refer to Appendix D for operating instructions and pinout.

Simple divide-by-four operation is achieved by connecting Output 4 (O4) to the Master Reset. Subsequently, the Master Reset clears the counter to zero which produces a "high" at Output 0. Figure 3-9 is a timing diagram showing the clock pulses from pin 7 of the 1 KHz multivibrator, the Master Reset,and the outputs, O0,O1,O2 andO3. Thus, the Johnson Counter produces a discrete one-of-four output.

JFET Gate Isolation

A basic analog gate is shown in Figure 3-10. This circuit provides the isolation desired between drive signal and switched signal without the use of transformers (Ref. 21:125). Since no offset voltage is present on the gate, it is possible to transmit signals on the order of microvolts. When the JFET should be off, the diode is biased so that the gate of the JFET is clamped to some turn-off voltage more negative than the pinch-off voltage. When the JFET should be turned-on, the diode is reverse biased, allowing the gate to float and allowing full conduction in the channel. Since the reverse biased diode represents a very high impedance, the JFET will remain off unless a path is provided to the gate for current to discharge the junction capacitance.

Figure 3-8 Johnson Counter

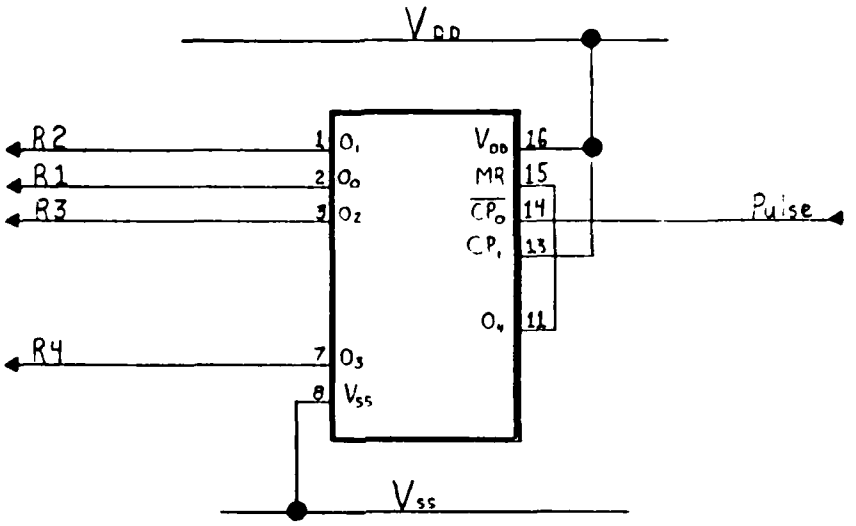


Figure 3-9 Timing Diagram

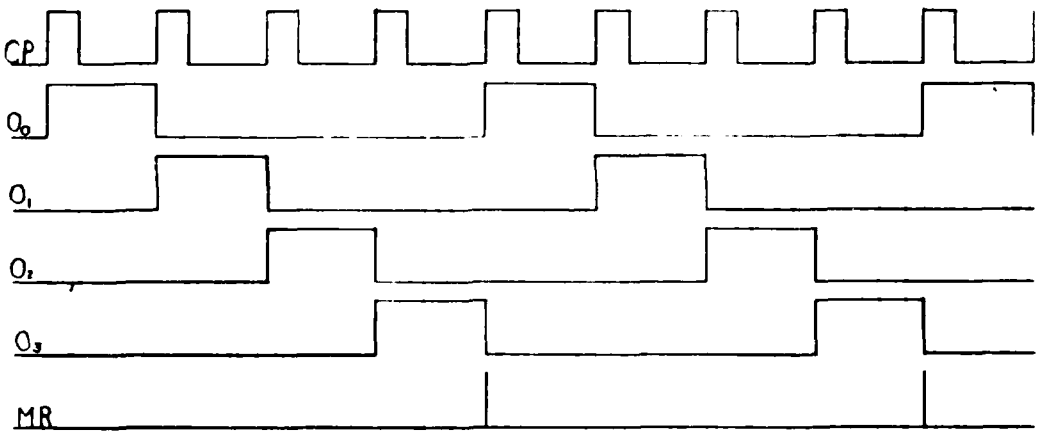


Figure 3 - 10

Simplified Gate Isolation

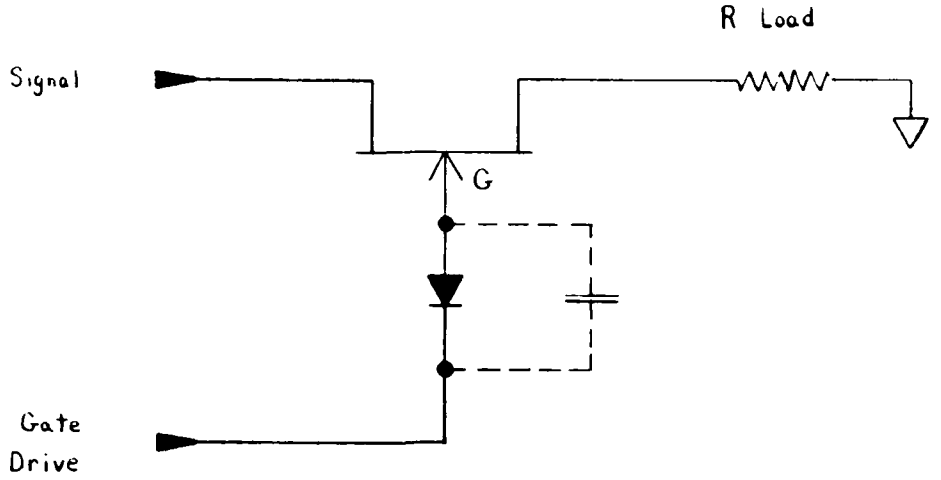
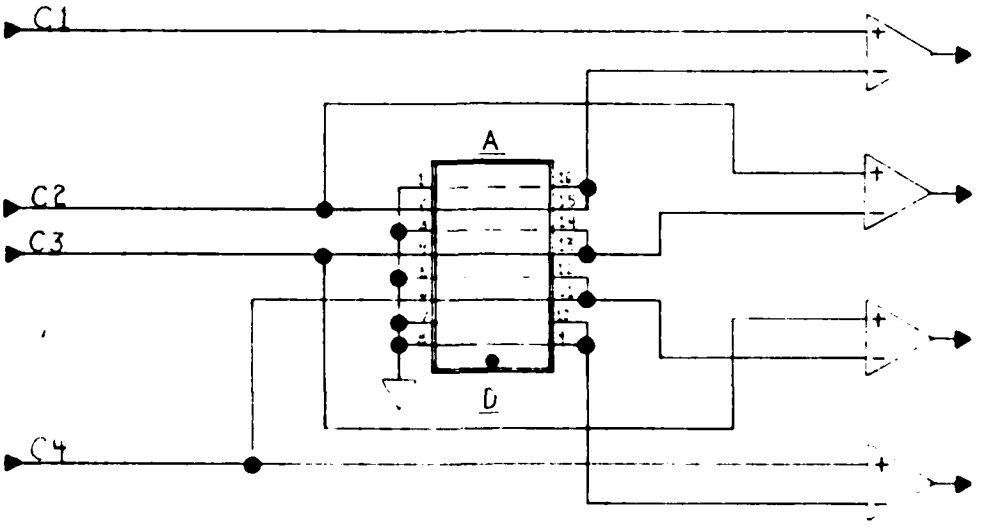


Figure 3 - 11

Ouput Voltage Measurement Method



A capacitor may be placed in parallel with the diode to supply this current (shown with dashed lines in Figure 3-10). In this case, however, the junction capacitance of the diode is adequate and a parallel capacitor is not required. A JFET is a two-way switch, thus designation of drain or source in Figure 3-10 is irrelevant.

Output Voltage Measurement Method

There are fundamentally only two ways to measure voltage: absolute or differential. In the absolute case, a voltage is measured with respect to the circuit reference. In the differential case, a voltage is measured with respect to another voltage, not the circuit reference. The external drive circuit must provide the ability to conveniently switch between these two methods.

Figure 3-11 shows how a dual-in-line-package (DIP) socket and a DIP component holder are used to provide this switching capability. The DIP component holder has a dot painted on one end. When the dot faces the D (for differential), the solid lines indicate connections providing differential measurement at the output terminals. If the dot faces the A (for absolute), the dashed lines indicate connections providing absolute measurement at the output terminals. Figure 3-12 is a simplified drawing of the circuit connections for absolute voltage measurement. Figure 3-13 is a simplified drawing for differential circuit measurement. Note that connection to differential amplifiers is assumed.

Figure 3-12

Absolute – Voltage Measurement

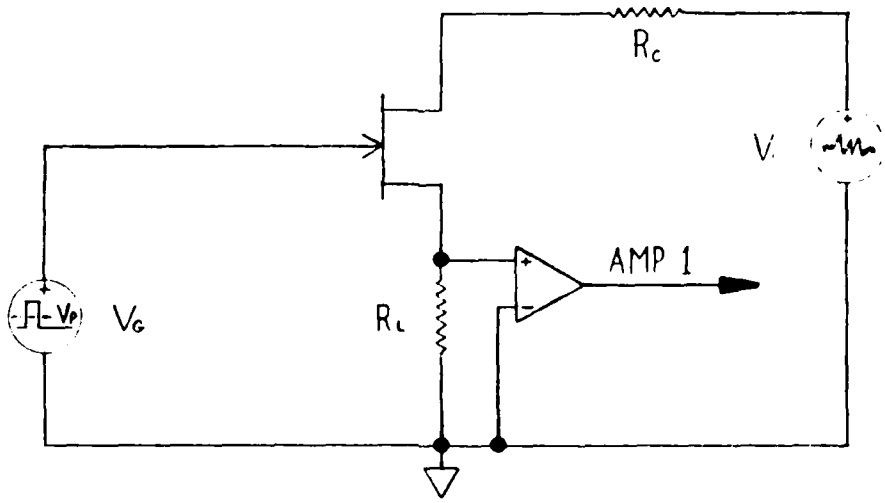
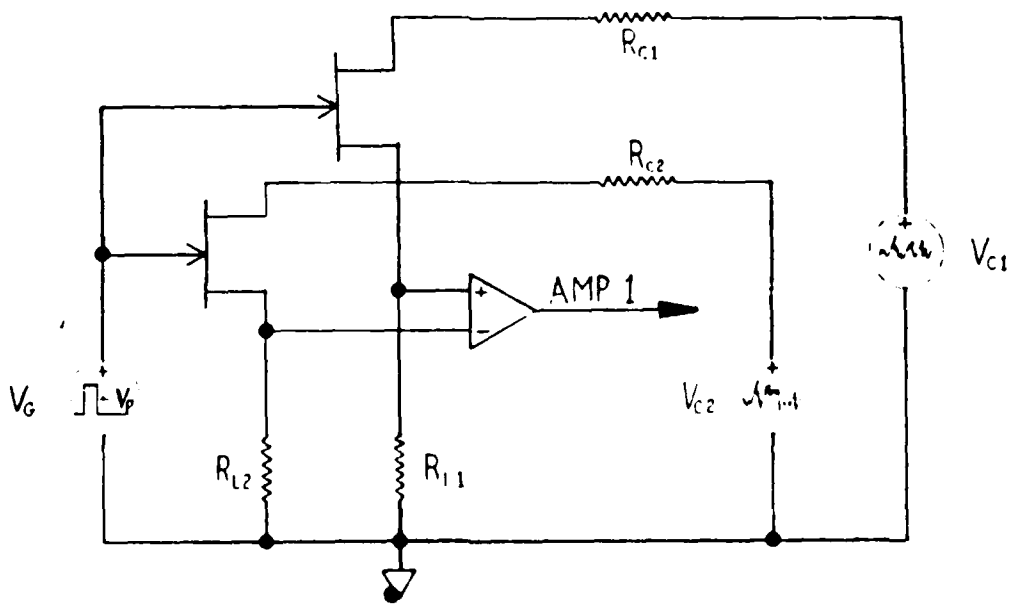


Figure 3-13

Differential – Voltage Measurement



Independent Operation

For the external drive circuit to operate independent of the AFIT multielectrode array, it must contain a circuit which performs or emulates essentially the same task as the AFIT array. Such a circuit is shown in Figure 3-14. JFET's Q1 - Q4 have operating characteristics very similar to those of the AFIT multielectrode array. As a result, signals passed through these JFET's produce outputs which are very similar to those of an AFIT multielectrode array. Switches S3- S6 direct the row drive pulses either to the internal JFET's (independent operation) or to the AFIT array.

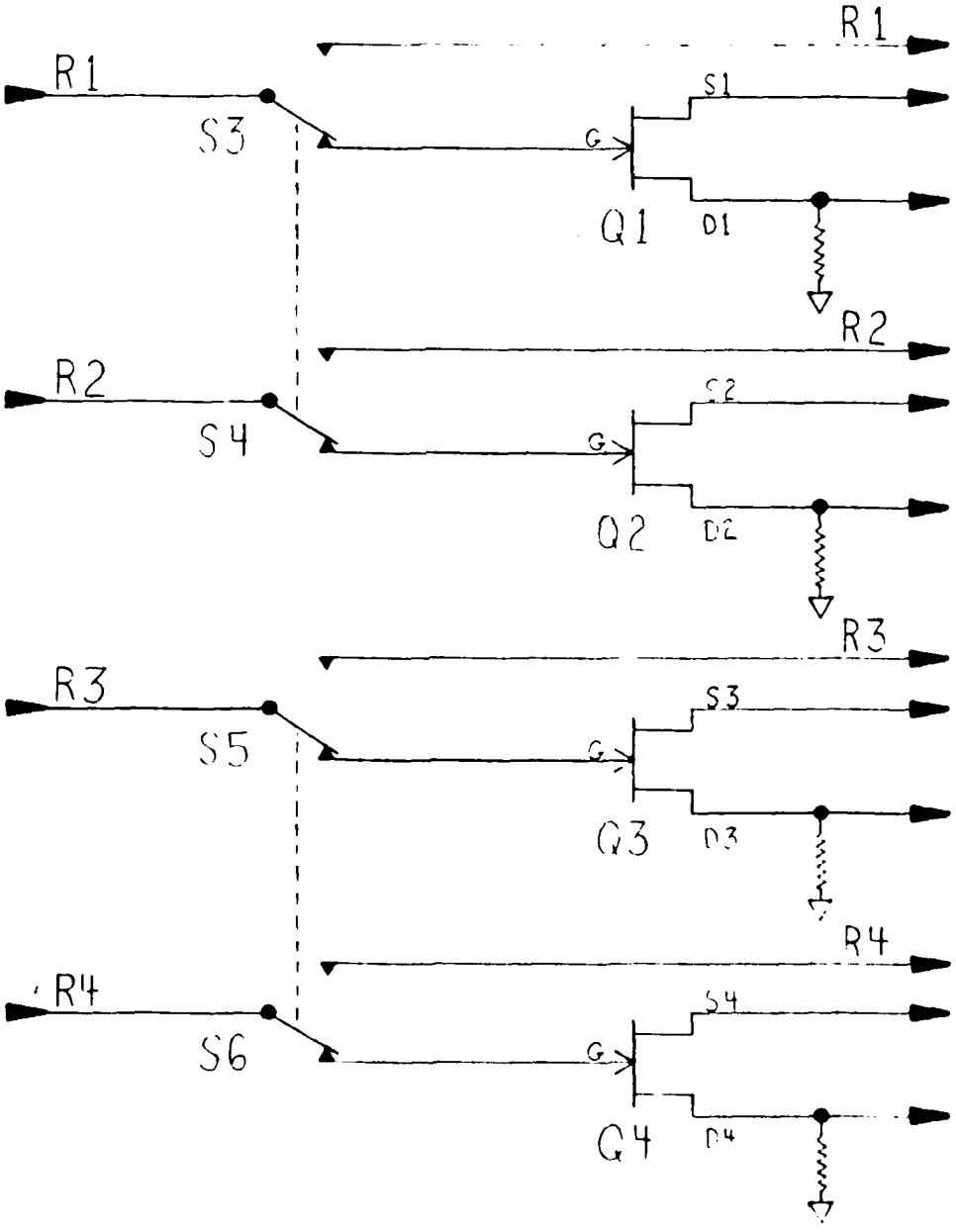
Each column output of the AFIT array represents one of four possible JFET's, thus it is possible to emulate operation of the AFIT array with one JFET per column. Therefore, application of row drives 0-3 to JFET's Q1-Q4 emulates output switching of the AFIT array. More specifically, output signals appear as shown in Figure 3-3. The AFIT array would yield this condition if an input signal were applied to only one JFET in each of the four columns.

JFET Compensation

Each of the sixteen discrete JFET's on an AFIT multi-electrode array may exhibit unique operating characteristics. There may be substantial variation in pinch-off voltage (Vp) and the off-resistance (R-off) of JFET's on the same chip. The most noticeable complication of this condition is the presence of a DC offset in the output signals. Were there only one DC offset present in

Figure 3-14

Internal JFET's



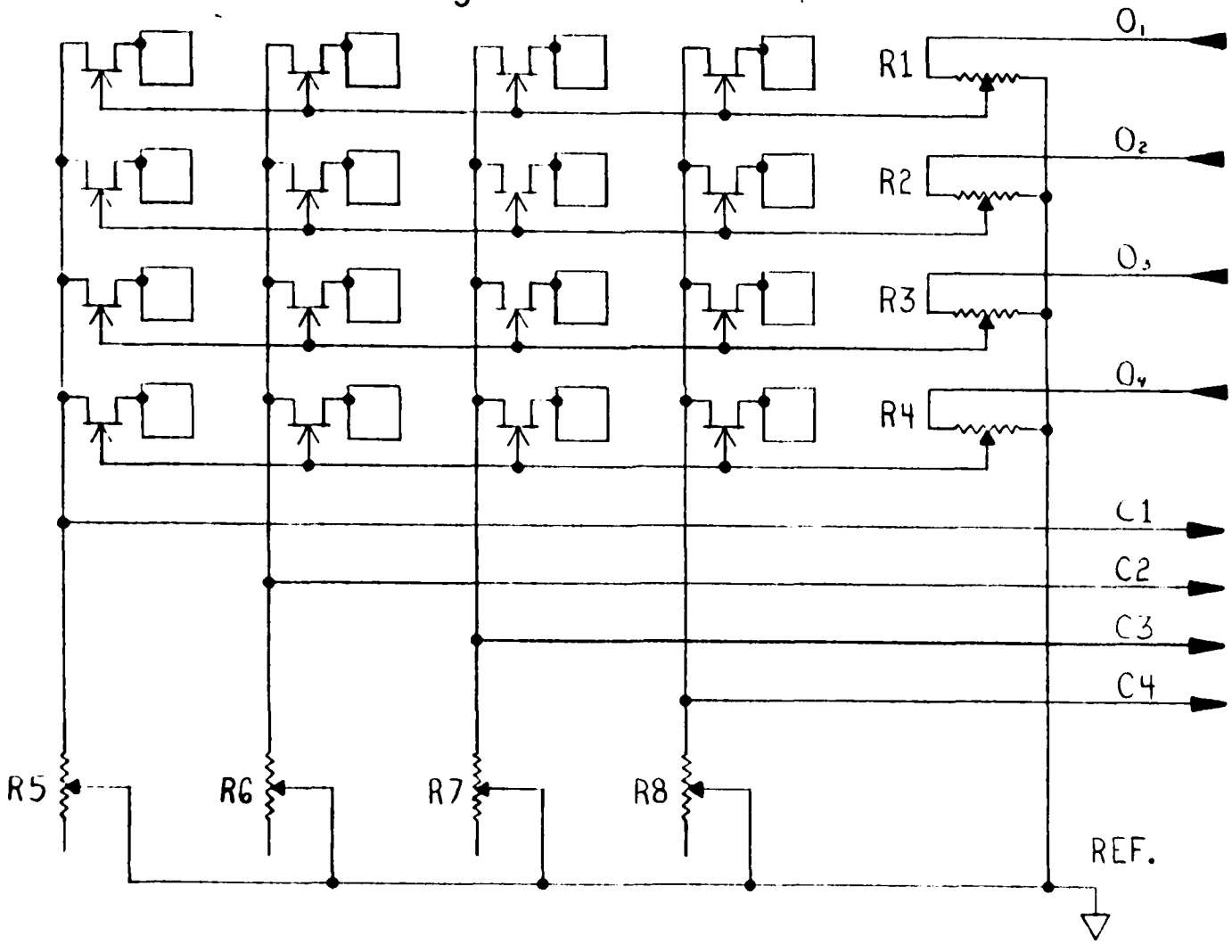
all sixteen output signals the solution would be trivial. Unfortunately, each JFET injects a unique DC offset into the multiplexed output. Also, each discrete offset may vary significantly from others.

Figure 3-15 shows how reasonable compensation is obtained. Output one (O1) is applied to variable resistor R1. Adjustment of R1 varies the amplitude of the pinch-off pulse applied to all the gates of one row. As a result, the off-resistance of the JFET's in this row can be modified. The same is true for rows two, three and four. Compensation among rows is obtained by adjusting the row drives for minimum DC offset.

At any discrete moment in time, only one JFET in a given column is turned on. Thus, there are four possible values of on-resistance in series with each column load resistor. When an AC signal is applied to the source of all sixteen JFET's, ideally, all sixteen output signals developed across the four load resistors should be the same. But, since there are sixteen different values of on-resistance, the output signals are not the same. Fortunately, there are only minor differences in on-resistance values. Thus, adjustment of the load resistors permits satisfactory compensation among columns.

It should be noted that complete adjustment of an AFIT array is not a trivial procedure. Proper alignment requires a four-channel oscilloscope to display the four column outputs. Also, the absolute voltage measurement method must be used. This is accomplished by setting a DIP

Figure 3-15 Compensation



"component-holder" to the "A" (Absolute) position. Next, the gate voltages of each row must be adjusted to minimize the difference between reference and the DC offset in each column. This is an interactive process and requires several iterations. Finally, a signal of known amplitude (e.g. 10 millivolts) is inserted into the AFIT array and the load resistors are adjusted to obtain outputs of equal amplitude. Proper alignment is obtained when the four column output signals are of the same relative amplitude and each multiplexed column output is adjusted for minimum DC offset.

Visual Evoked Response Circuit

The Visual Evoked Response (VER) circuit is comprised of an MC14538B, Dual Retriggerable, Resettable Multivibrator and a miniature 5V DIP relay. Figure 3-16a shows how the two one-shots are functionally connected; Figure 3-16b shows the circuit timing diagram and Figure 3-16c shows an electrical diagram of the VER circuit.

Functionally, one-shot A (Pins 9-15) is in parallel with one-shot B (Pins 1-7). A switch-controlled "Clear" level is applied to both one-shots and both trigger on input B. However, the A input of both one-shots is connected to the Q output of one-shot A. This unique arrangement prevents retriggering of either one-shot until after the Q output of one-shot A returns low. The time constant of one-shot A determines a minimum period T and the time constant of one-shot B is the "on-time" when relay K1 is energized. The Q output of one-shot B is the strobe signal.

VER

Figure 3-16a Functional Diagram

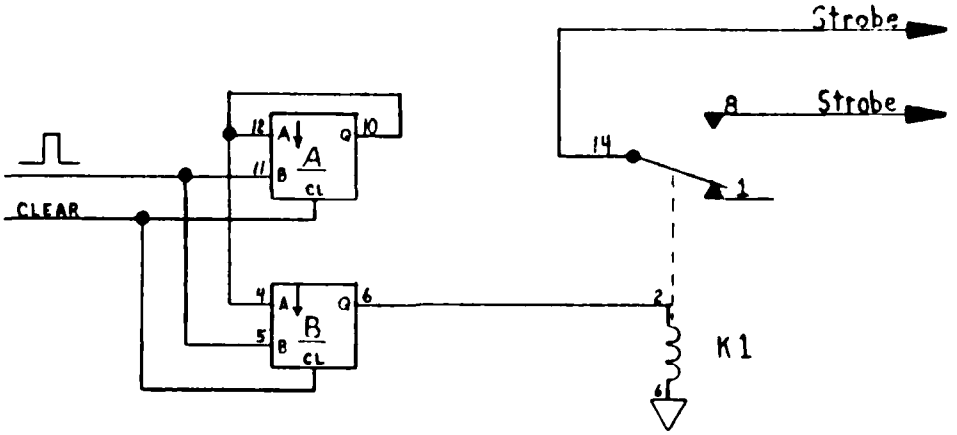


Figure 3-16b Timing Diagram

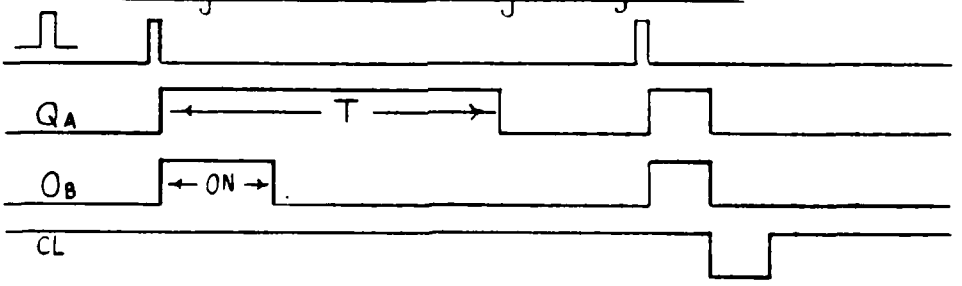
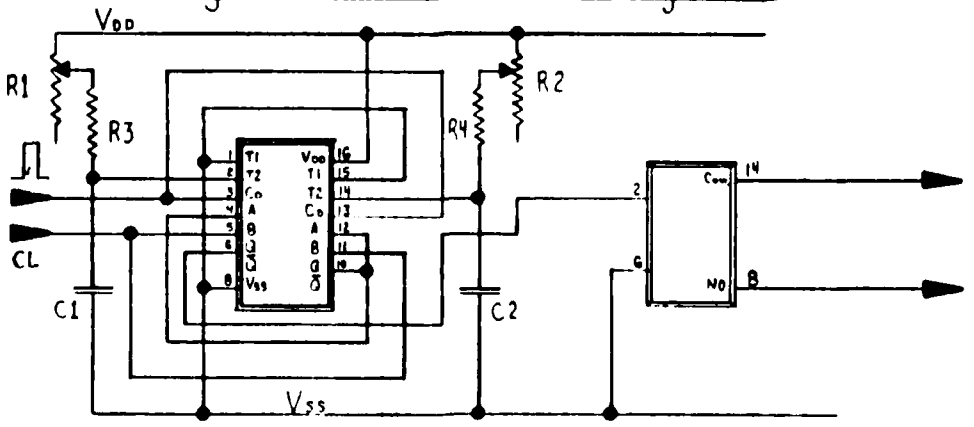


Figure 3-16c Electrical Diagram



CIRCUIT BOARD CONFIGURATION

Figure 3-17a shows the electrical diagrams and Figure 3-17b, the component layout of the external drive circuit board. In Figure 3-17b, note that columns on the circuit board are labeled A and B. Rows are labeled one through five. For example, relay K1 is at position A5 on the circuit board. A component designation (i.e. R1, C1, K1, etc.) is shown for each component. Absolute or differential output is selected by proper orientation of the "component-holder" in DIP socket B4 (i.e. the dotted end reflects the type of output desired: "A" for absolute, "D" for differential). Table 3-1 lists components required for each external drive circuit board.

A duplicate circuit board was also fabricated to provide back-up capability. If the operating circuit board fails the duplicate board may simply be substituted for the defective circuit board.

Figure 3-17a

External Drive Circuit Board

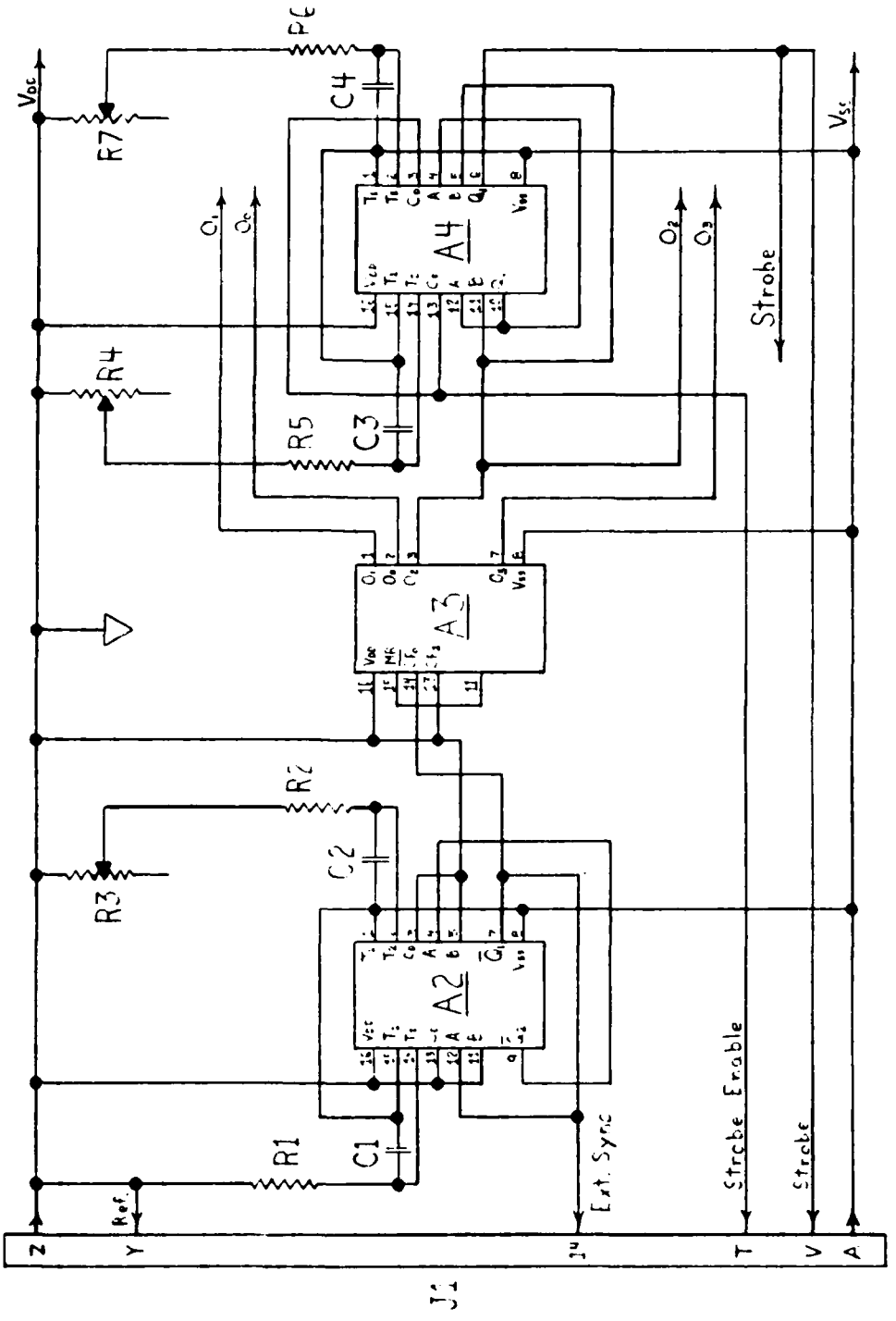


Figure 3-17a

Circuit Board Cont.

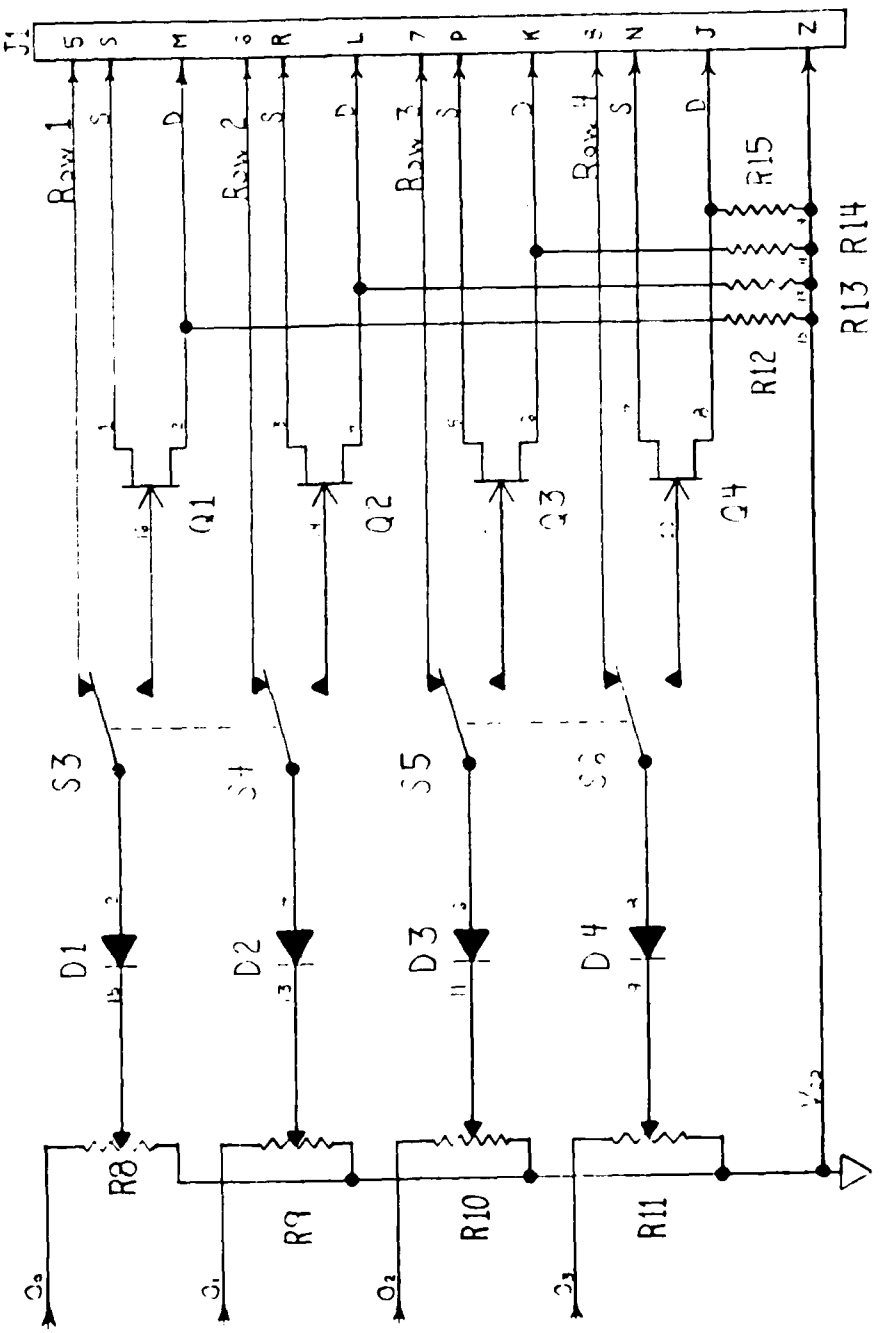


Figure 3-17a

Circuit Board Cont.

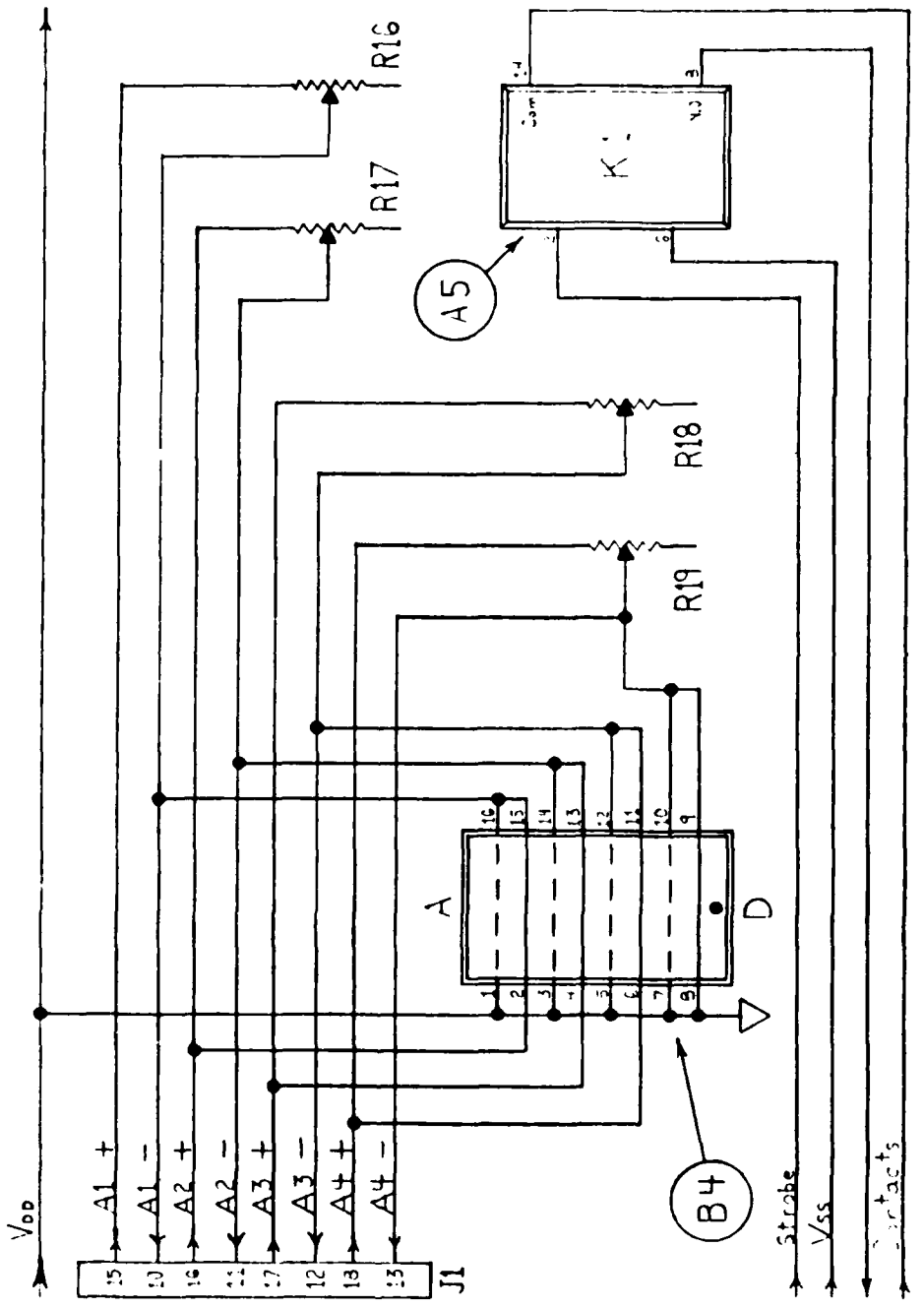


Figure 3-17b

External Drive Circuit Board Layout

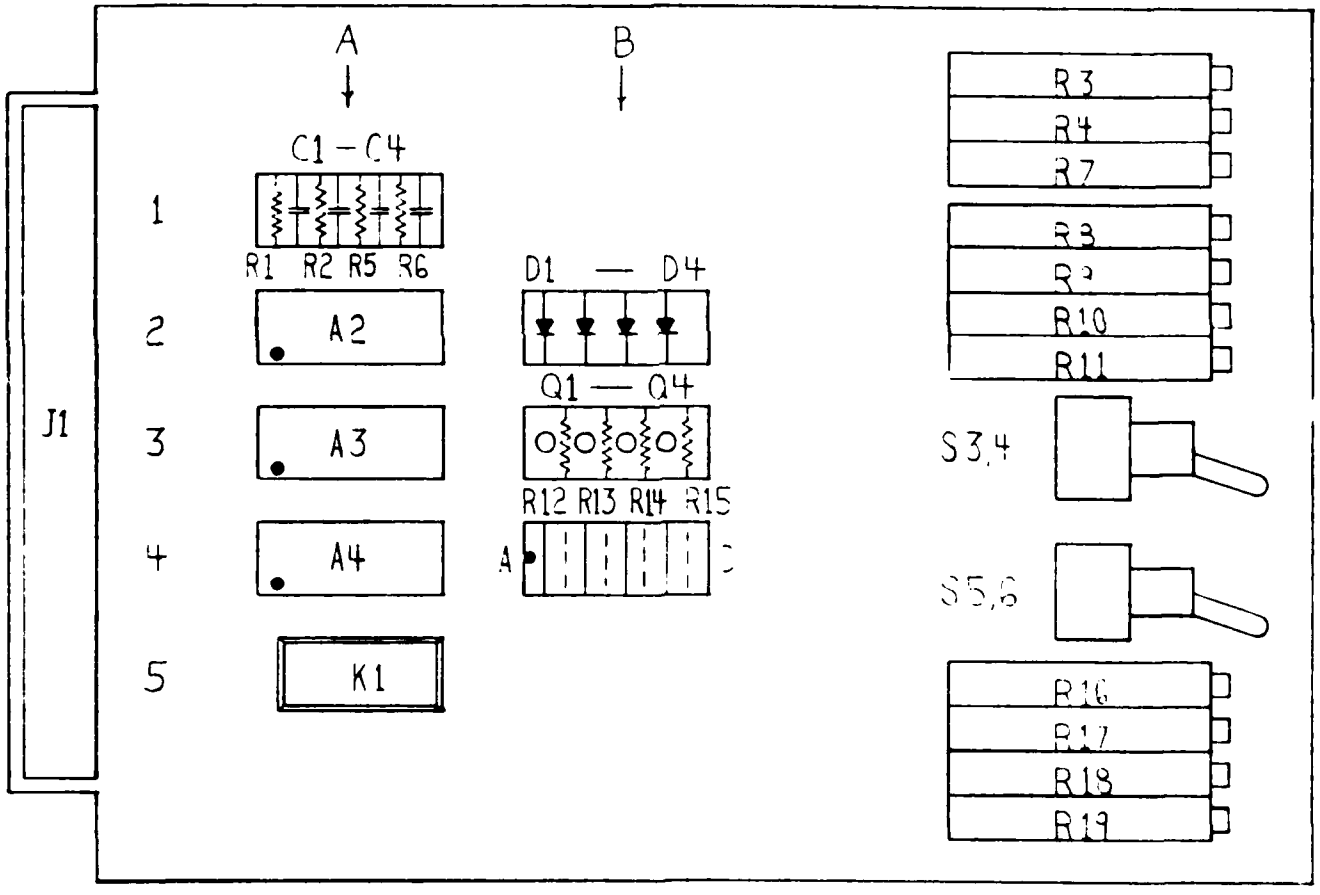


TABLE 3-1

EXTERNAL DRIVE CIRCUIT BOARD

COMPONENTS

A1,A3		MC14538B
A2		MC14022B
S3,S4	DPDT PC SWITCH	JBT-T02-221
S5,S6	DPDT PC SWITCH	JBT-T02-221
Q1-Q4	JFET	2N4393A
D1-D4	3.6V ZENER DIODE	1N747
K1	CLARE REED RELAY	PRMA1A05
BOARD	DIP PLUGBOARD CUT TO 6" LENGTH MATES WITH R644	3682
EJECTOR	CARD EJECTOR	SCAMBE 203
SOCKET	16 PIN DIP SOCKET	8 ea.
COMP. HOLDER	COMPONENT HOLDER	4 ea.
C1	.001uF 10V DISC	
C2	.01uF 10V DISC	
C3,C4	.47uF 10V DISC	
R1	110 KOHM 1/4 W	
R2	47 KOHM 1/4 W	
R3	20 KOHM 1/2 W	VARIABLE CERMET
R4,R7	500 KOHM 1/2 W	VARIABLE CERMET
R5	820 KOHM 1/4 W	
R6	39 KOHM 1/4 W	
R8-R11	10 KOHM 1/2 W	VARIABLE CERMET
R12-R15	5 KOHM 1/4 W	
R16-R19	10 KOHM 1/2 W	VARIABLE CERMET

EXTERNAL DRIVE CIRCUIT CHASSIS

Figure 3-18 shows various views of the external drive circuit chassis. Refer to Appendix E for chassis mechanical drawings. The chassis provides slots for two circuit boards. The upper circuit board slot is functional and the lower circuit board slot is a spare.

Four size "AA" batteries in series provide 6 Volts. The positive terminal of the battery holder is defined as VDD, zero volts, and is often referred to as "common" or "reference". This potential is applied to the chassis and the reference electrode of the AFIT multielectrode array. The negative terminal of the battery holder is defined as VSS, -6 Volts, and is only applied to the integrated circuits and relay.

Figure 3-19 is a chassis and cabling diagram. J1 is a 44-pin connector to the external drive circuit board. J2 is a 44-pin connector to the spare circuit board. Note J2 is not found on Figure 3-19 since there are no electrical connections to it. J3 and J4 connect the external drive circuit to the AFIT multielectrode array. J4 is the connector at the AFIT array. J5 permits connection to an external strobe light. J6 through J23 are "BNC" connectors to many output functions.

Although it is not clear from Figure 3-19, a cable with nine coaxial conductors exists between J3 and J4. The shields of the coaxial cables are connected to reference through J3 pin 5. However, the shields are not connected at

J4. Thus, reference is used as a shield for the AFIT array signals.

FIGURE 3-18a

EXTERNAL DRIVE CIRCUIT CHASSIS

(FRONT VIEW)

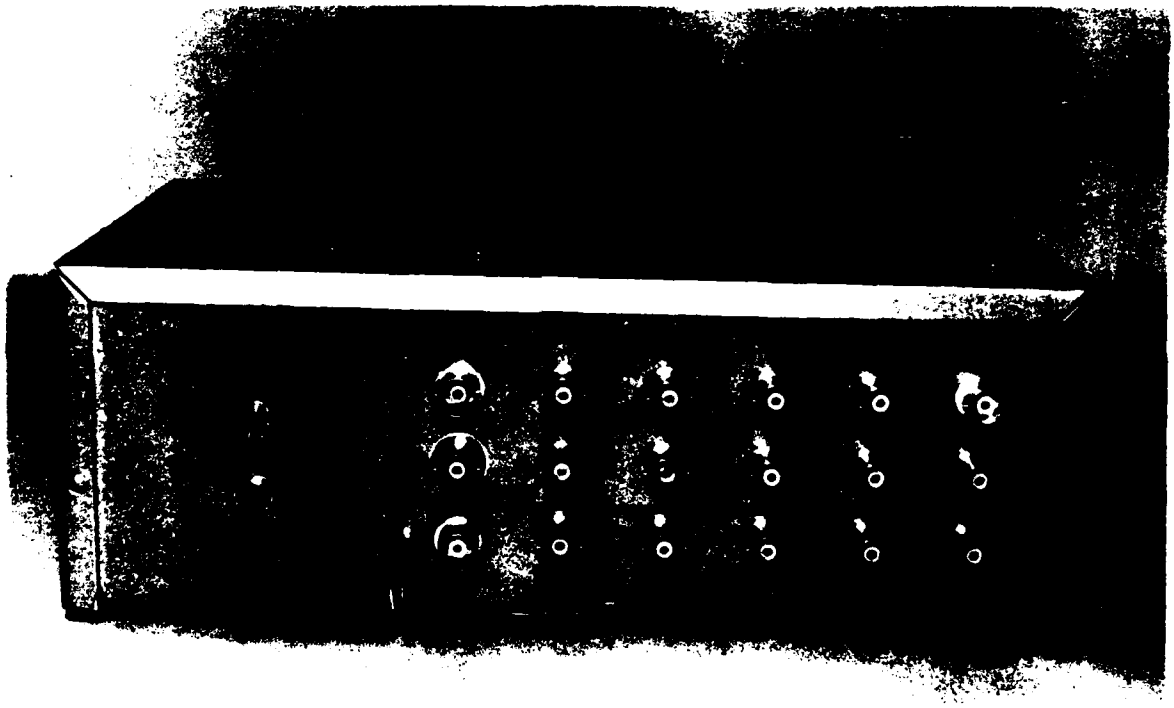


FIGURE 3-18b

EXTERNAL DRIVE CIRCUIT CHASSIS

(SIDE VIEW, OPEN)

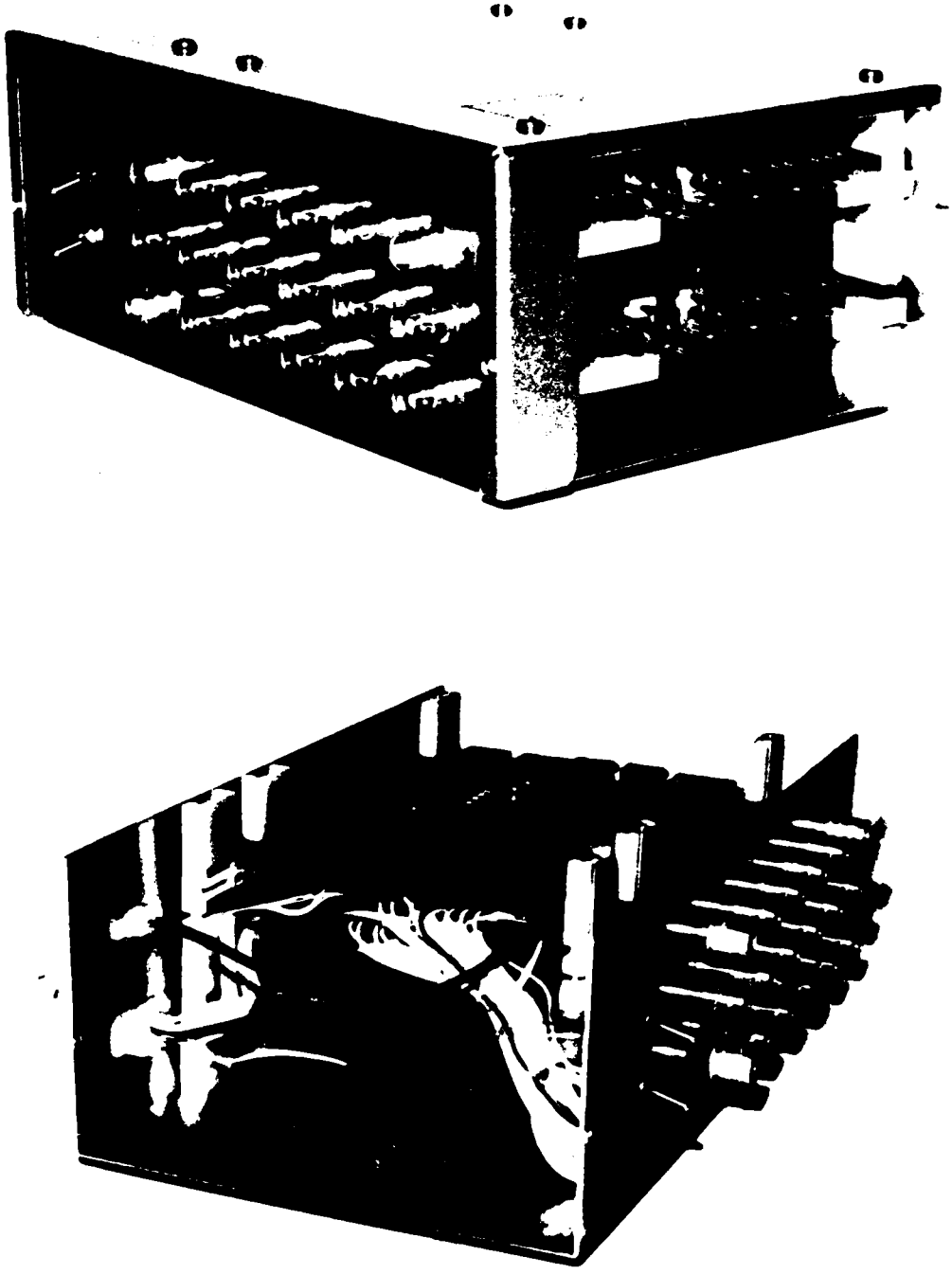


Figure 3-19

Chassis + Cable Wiring

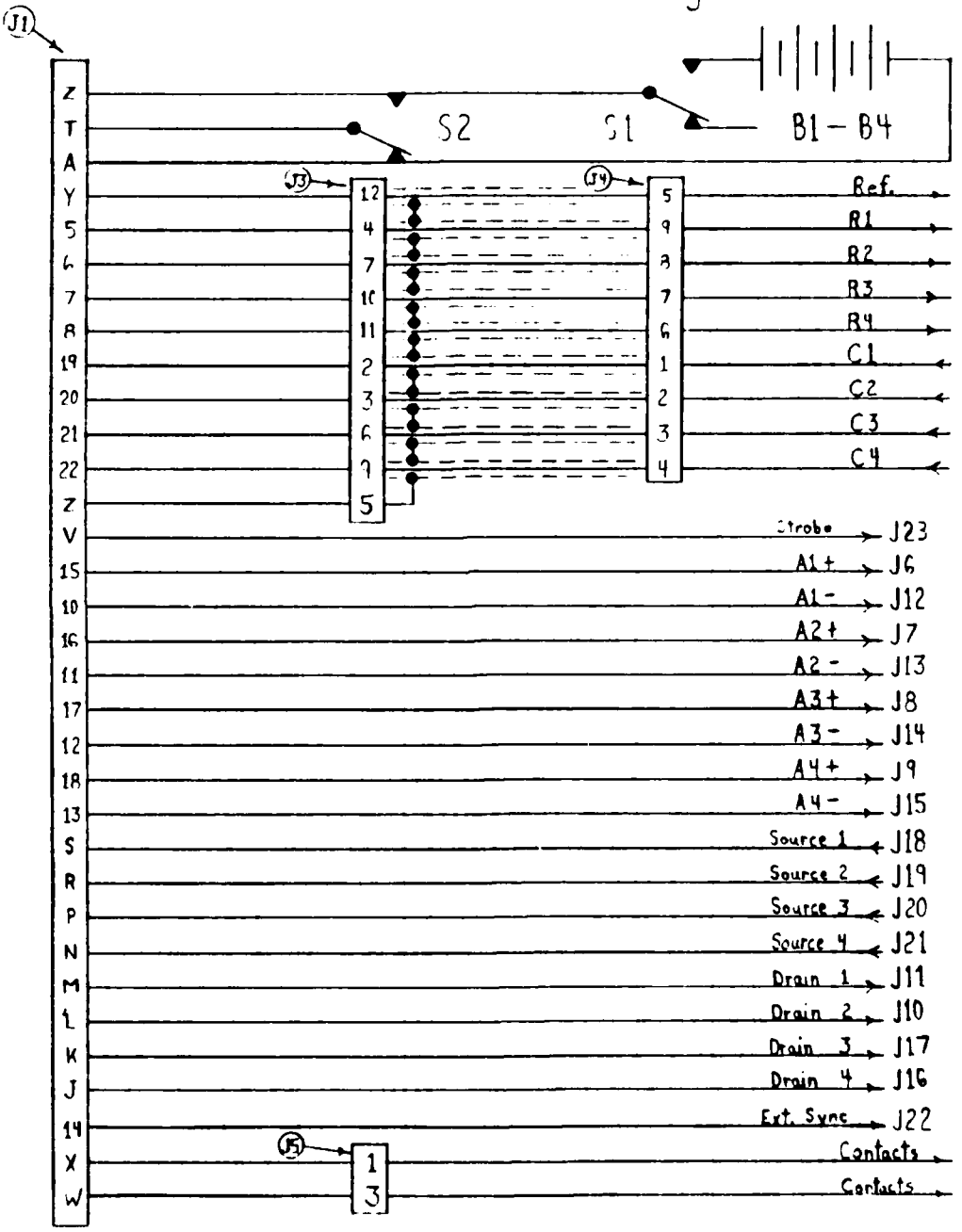


Table 3-2 is a chassis parts list. All parts necessary to build the chassis are listed except the card cage. There are several commercial methods of implementing a printed circuit board card cage. The method used will only affect locations of the mounting holes. However, it is important that there be provision for two circuit boards (i.e. the functional board and the spare). Rubber feet are necessary to provide isolation from other surfaces.

TABLE 3-2

EXTERNAL DRIVE CIRCUIT CHASSIS

PARTS LIST

J1	EDGE CONNECTOR (TOP)	R466
J2	EDGE CONNECTOR (BOTTOM)	R466
J3	12 PIN MOLEX PLUG	03-06-2121
	RECEPTACLE	03-06-1121
J4	9 PIN MOLEX PLUG	03-06-2091
	RECEPTACLE	03-06-1091
J5	5 PIN MOLEX PLUG	03-06-2031
	RECEPTACLE	03-06-1031
J6-J23	BNC CONNECTOR	30220-1
S1,S2	SPDT, 0.1 AMP, 10 VOLT MINI SWITCH	7103SYZQE
BOX	BUD, GRAY ALUMINUM	CU2110-A
BATTERY	4 ea. "AA" CELLS	
HOLDER	BATTERY HOLDER HOLDS 4 "AA" CELLS	
CARD CAGE	AS REQUIRED	
FEET	RUBBER, 4 ea.	

CHAPTER IV

SYSTEM INTEGRATION AND ARRAY TESTING

SYSTEM INTEGRATION

The AFIT Multielectrode Array requires a support system capable of providing a synchronized visual stimulus, extremely high amplification, and recording capability. In addition, such devices as a signal generator and oscilloscope are required for alignment of the external drive circuitry.

Since this type of experiment has never before been attempted, the exact type of signal and signal amplitude to be extracted from the cortex was unknown. However, 25 to 40 microvolts was expected (Ref 18:360). A high signal-to-noise ratio and a gain of at least 1000 are required to amplify these signals to recording levels. Such requirements mandate the use of a differential input amplifier; a Princeton Applied Research 113 (or PAR 113) is such an amplifier. The AFIT Array support system required a total of five PAR 113 amplifiers; an amplifier for each column output and one additional amplifier for an indifferent scalp electrode.

The PAR 113 is capable of battery operation, thereby reducing the effects of 60 Hertz noise. Its very high common-mode-rejection-ratio also reduces the effects of noise and permits amplification factors of up to 10,000. It is possible, however, to overload the PAR 113 on any scale if the output exceeds plus or minus twelve volts.

The amplifier output also incorporates both low frequency and high frequency filters.

The tape recorder used in the AFIT Array support system must have at least eight channels; five for amplifier signals, one for an external sync signal, one for the strobe signal and one audio channel. The audio channel is absolutely necessary for documenting the condition of the system (connections, gain and filter settings, etc.) and other particulars such as the date, time, condition of the subject and type of test being conducted. The audio channel also serves as a continuous event marker during testing.

It is very important to check the amplitude and frequency response of each tape recorder channel before tests begin. (SPECIFICATIONS IN THE OPERATING OR MAINTENANCE MANUALS CANNOT BE TRUSTED!!) Each channel must be tested. Specifically, the maximum and minimum signal levels that each channel can record and reproduce without distortion must be determined. The noise level of each channel must also be identified (i.e. 60 Hz, high frequency, ringing, etc.).

The experiment requires a visual stimulus. Therefore, the AFIT array support system incorporates a "white-light" strobe synchronized by the external drive circuitry. Visual evoked response calculations require the strobe signal to be recorded. However, because the strobe signal exceeded the tape recorder input limit, an in-line voltage divider was necessary to reduce the strobe signal to recording levels.

Alignment of the AFIT Array support-system requires at least one signal generator. The signal generator must be capable of generating low frequency (0 to 50 Hz), low amplitude (microvolt) signals. Additionally, alignment signals must not have a DC offset. Alignment of the suppport-system also requires a high quality 4-channel oscilloscope. A Tektronix 7000 series mainframe and high-gain vertical amplifiers were used in this experiment.

SYSTEM INTERCONNECTIONS

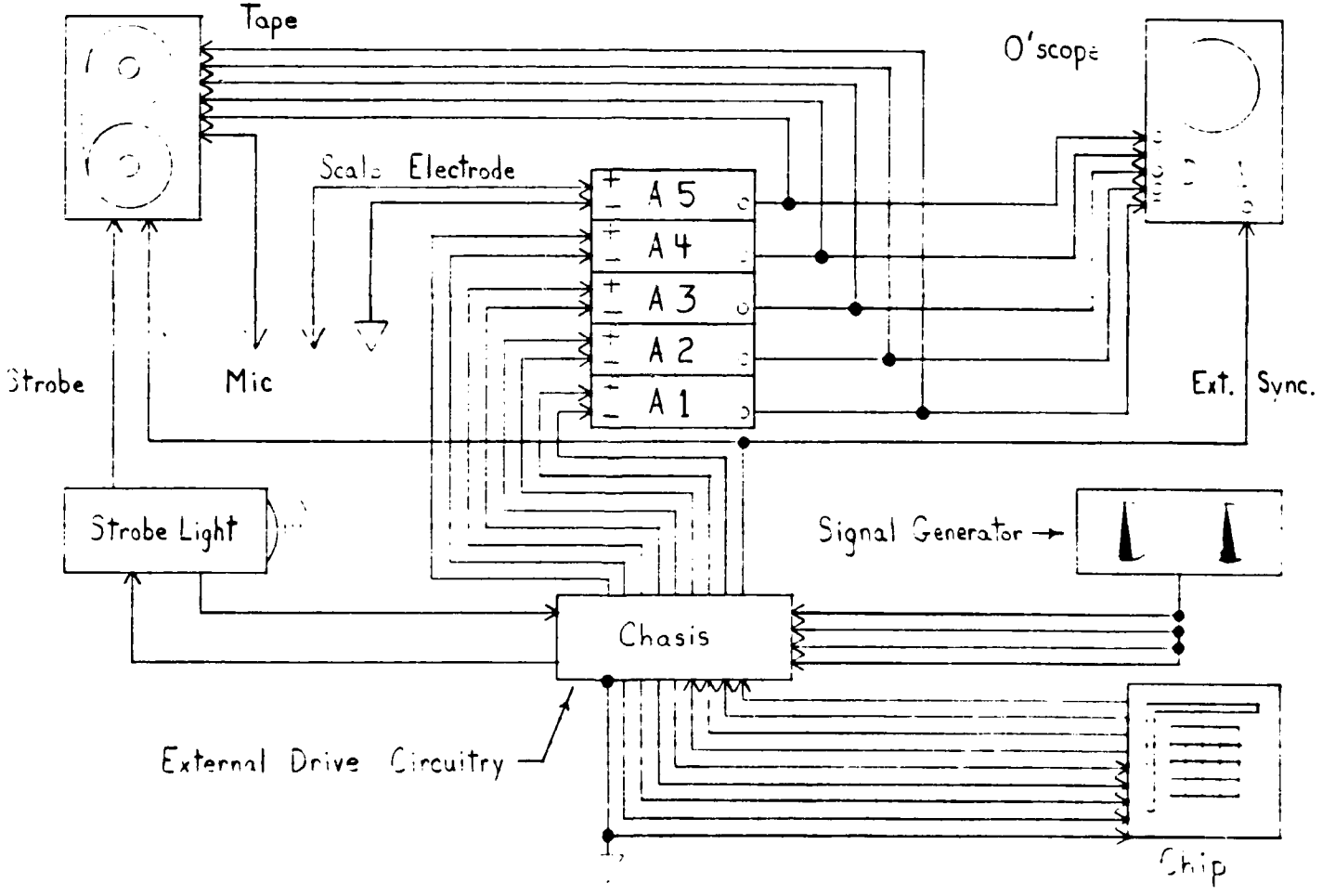
Figure 4-1 shows the connections necessary for operation of the AFIT Array. This system requires a nine (coax) conductor cable between the external drive circuit chassis and the plug of J4 connected to the AFIT Array. An additional twenty-seven to thirty coaxial cables with BNC connectors are necessary.

The cable from the external drive circuit to the array connector, J4, consists of nine small gauge coax wires. Coax is used to provide shielding for the microvolt signals being conducted from the probe. The shields of these nine coaxial wires are connected to the external drive circuit chassis only.

The shields of all other coaxial cables may be attached to the BNC connector at both ends. However, caution must be exercised to prevent ground loops within the system. The noise produced by ground loops in this system could be greater than the cortical signals, an intolerable condition.

Figure 4-1

System Interconnections



AFIT Array Connector

A temporary connection from the external drive chassis to the AFIT Array was made through a Molex nine pin plug and receptacle (J4) (see Figure 3-19). The plug was only temporarily connected to the AFIT Array for purposes of testing and initial alignment. Later, the plug was removed. It was much easier to sterilize and implant the probe assembly (encapsulated AFIT Array and conductors) with plug J4 removed. During implant, it was necessary toliterally pull the array wires under the animal's skin from the skull area to a point between the shoulder blades. With the plug, J4, attached, it would have been difficult.

Prior to removing the array wires from J4 (plug) it was essential to label each one. Once the AFIT Array and wires are encapsulated it is not possible to determine the point where each wire contacts the array. Therefore, a method of wirelabeling must be devised which is reliable and permanent. For this experiment, a length code was established and wires cut to length. After the probe is implanted, it is necessary to reconnect the plug of J4. This was done in the operating room immediately after the wounds were sutured.

SYSTEM TESTING

Before testing an AFIT Array, operation of each system component must be checked. More importantly, the wiring and performance of the entire support system must be evaluated. Operational system tests were facilitated by the ability to

operate the external drive circuit independently.

Independent System Tests

With four different signal generators connected to the source inputs of the external drive circuitry, and the drains connected to the amplifier inputs, the oscilloscope was used to perform a channel by channel test of the amplifiers and tape recorder. Amplifier A5 and it's tape channel were checked separately, as was the audio channel.

Operation and synchronization of the strobe light was also tested.

System Testing With The AFIT Array

Chapter II discussed preliminary tests conducted to verify polyimide as a viable encapsulant. Once a potentially implantable probe had been processed, similar testing was required to verify proper operation of the probe and the integration of all system components supporting the probe. Also, this testing would identify the length of time a potentially implantable probe could survive in a CSF simulated environment.

To initiate this testing the drive circuit had to be switched to the external mode and the test probe connected to it. Once the drive circuit and other system components were set the probe was placed onto the simulated cortex discussed earlier. In this test, the moisture of the "brain" was maintained by dripping a saline solution into the tray.

A life expectancy was discussed in chapter II and there were reasonable grounds to suspect this probe would survive at least as long as the initial test probe. Unlike the method used to determine those JFET's which were functional on the preliminary test array, an individual test of each JFET on an implantable array risked damage to the probe. Therefore, the functional aspect of the JFET's was observed when the probe was placed in the simulated CSF. Fortunately, all sixteen JFET's were functional even though they exhibited different operating characteristics.

A signal was induced across the "simulated-brain". After placing the probe in the solution, the desired observation was sixteen separate signals similar to that depicted in chapter III (Figure 3-3). This would indicate proper operation of the drive circuit and a potentially implantable array. This was in fact observed when the signal induced across the "simulated-brain" was on the order of one volt peak-to-peak. However, it must be noted that most of the integration testing with an external array was conducted without the PAR 113 bio-amps in the system configuration. Because the PAR 113 amplifiers had not yet been modified for battery operation, they induced 60 Hz noise into the signal stream. This characteristic had been noted earlier when the PAR 113's were checked and therefore, they were excluded from the array tests.

Omission of the bio-amps presented another problem. Since the signal being sampled by each JFET was essentially the same, it was impossible to draw any conclusions

regarding differential operation. There was also some concern whether or not expected cortical signal levels could be sensed by the probe (i.e. microvolts). Without the bio-amps such a determination could not be made. A good indication was obtained by reducing the output of the signal source to minimum and observing that the oscilloscope trace showed the presence of a signal.

Another item of importance is the quality of the sampled signal. The sampled signal was observed to be noise-free indicating neither the drive circuit nor the electrode introduced any noise into the signal. Because signals in the brain are on the order of microvolts, this observation was significant.

When the probe was first placed on the "simulated-brain", DC offsets present were minimized with compensation (chapter III). Although the JFET's could not be identically matched, the compensation brought the signals within microvolts of one another. Using this initial compensation as a base line, adjustments were made as required to keep the operating characteristics of the JFET's as close as possible to each other. The probe continued functioning with only minor adjustments required.

As previously mentioned, it was suspected that the probe would continue reliable operation for at least sixty hours. Instead the probe's characteristics became stable at the expected time of failure. This was a surprising result. A noticeable change in characteristics occurred after ninety

hours of testing. On the fifth day, after a continuous test time of over 100 hours, the probe failed. It was examined to determine the cause of failure. Although no distinct failure mode was observed, moisture absorption was the most probable cause of failure. Perhaps insufficient "cure" of the PI encapsulant permitted moisture to be absorbed. Another factor that may have contributed to the probe failure was discovered during probe examination. The initial preparation of the "simulated brain" involved saturating a pad of paper towels with a saline solution. Moisture was maintained by adding more saline solution, thus increasing the sodium concentration as the excess water evaporated. Even though the probe eventually failed, it far exceeded the expected operating period. A new probe was encapsulated and preparations were made for implant surgery.

CHAPTER V

IMPLANT (PREPARATION AND SURGERY)

This chapter is divided in two major sections. The first section discusses preparations for a surgical implant of the AFIT probe in a laboratory beagle. The second section is concerned with the actual surgery required to accomplish the implant.

Preparation

As previously noted, original plans called for the implant to be in a primate. At the beginning of this study conversations with personnel at the Air Force Medical Research Laboratory, Veterinary Sciences Division (AMRL/VS) indicated a primate would not be available for this study. However, a laboratory beagle was held for this work. Such a change dictated research into the visual areas of canines, specifically beagles. Figure 5-1 shows the visual pathways of vertebrates in general. Although the structure is basically the same in all vertebrates, the specific location of visual cortex may differ.

Figure 5-2 shows the visual pathways of the dog in particular. However, the specific area of a beagle's brain corresponding to the visual processing regions had to be identified. Figures 5-3 and 5-4 show the topographic mapping of the beagle cortex.

FIGURE 5-1

VERTEBRATE VISUAL PATHWAYS
(Ref. 23:289)

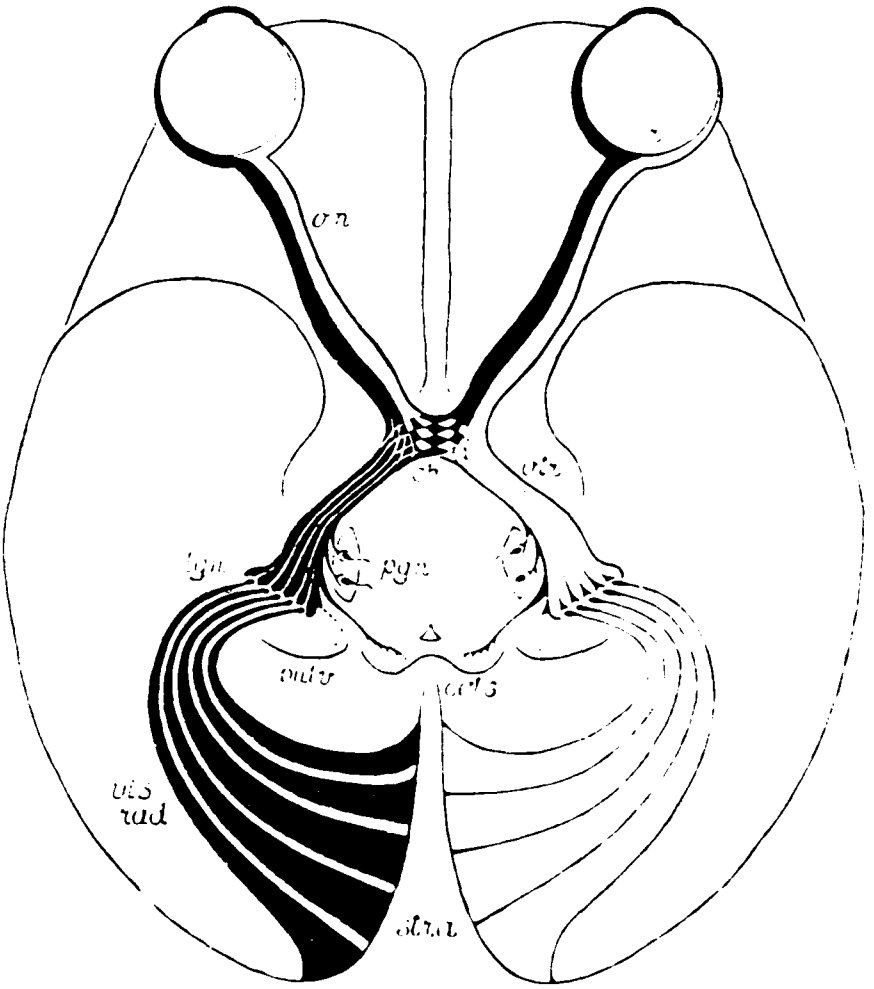


FIGURE 5-2

CANINE VISUAL PATHWAYS AND CORTICAL CORRESPONDENCE
(Ref. 23:151)

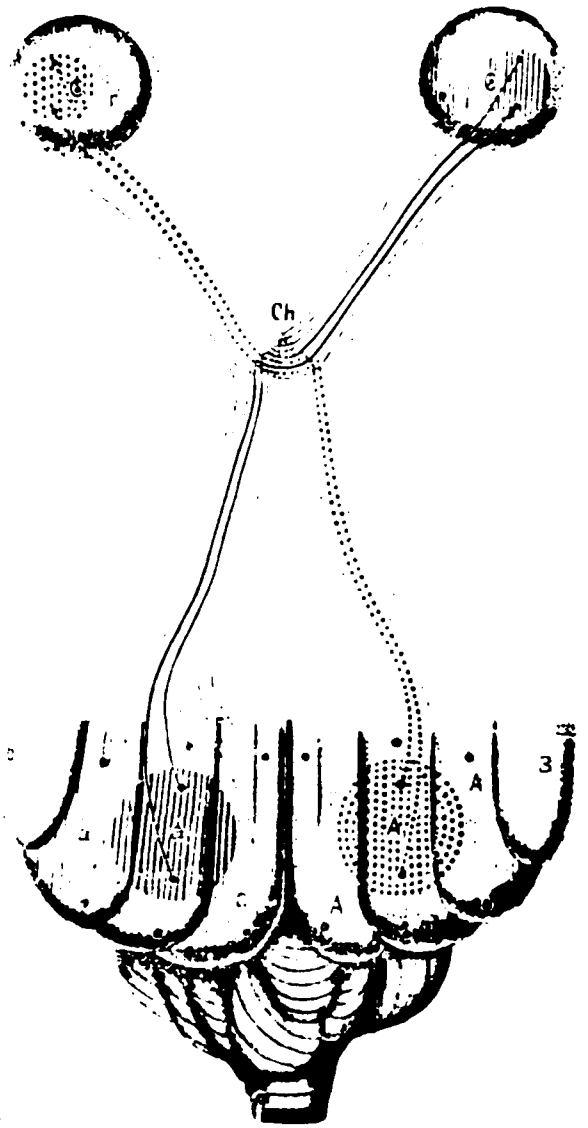


FIGURE 5-3

BEAGLE BRAIN; DORSAL ASPECT
(Ref. 18:351)

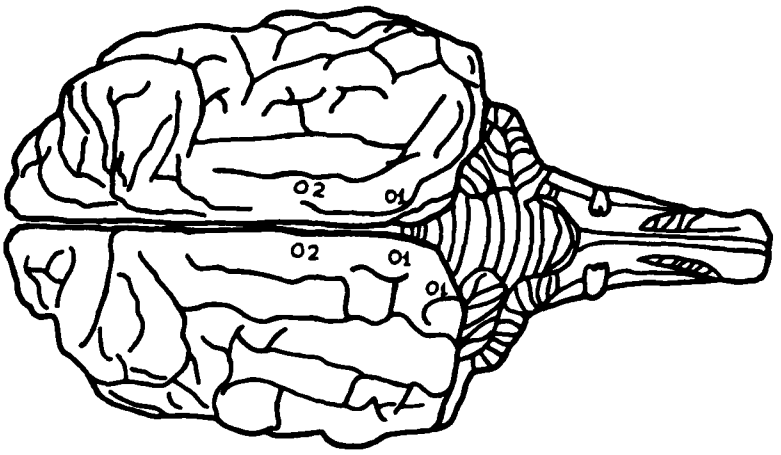
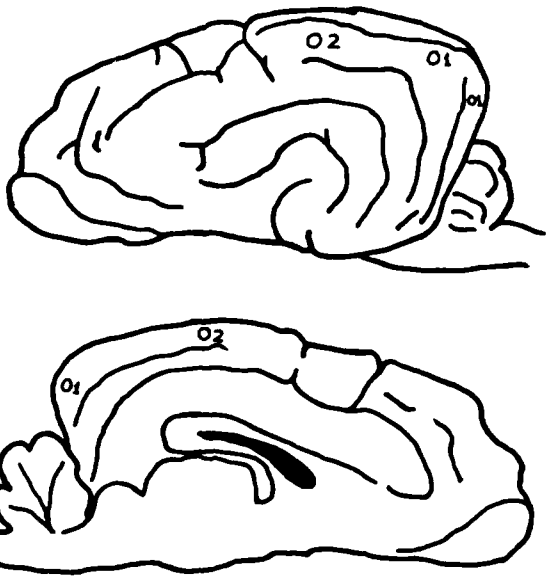


FIGURE 5-4

BEAGLE BRAIN; LATERAL AND MEDIAL VIEWS
(Ref. 18:354)



The areas labeled O1 and O2 (occipital 1 and occipital 2, respectively) are the areas of interest. O1 is the cortical region which receives signals from the eye first. O2 is the secondary processing region and receives data primarily from O1 (Ref. 3). These areas are also referred to as primary and secondary visual cortex, or area 17 and area 18, respectively. As the designation suggests, in the vertebrate there is an association between information processed in the two areas. However, nothing is known about the actual calculations performed by any animal capable of seeing and recognizing images. Hopes of eventually determining the transfer function from the homeomorphic mapping of the primary visual cortex to an association area (if such a function exists) motivated Tatman's original research (Ref. 5). At this point, having verified the probe and related system equipment, the objective was to successfully implant the probe and sample brain activity present at the sensing pads.

For the implant, the area of interest was O1. Figures 5-3 and 5-4 reveals that O1 is primarily on the dorsal area of the brain. This being the case, O1 was potentially inaccessible. The canine skull has a large bone protuberance, the external occipital protuberance, at the juncture of two bones. Additionally, the external sagittal crest is a potential problem (Ref. 22:44). This bone structure is thick and, if unavoidable, would present extreme difficulty during implant surgery. Research indicated that the probe could be implanted without

interference of either the external sagittal crest or the occipital protuberance while still placing the probe in the desired area.

A second potential problem arose in gaining access to the cortex through the skull and protective membranes. While it is desirable to make the cranial opening as small as possible, the opening must be large enough to permit retraction of the protective membranes. These membranes are tough and inelastic, thus the smaller the opening, the more difficult it would be to place the probe on the cortex.

Besides the items already covered, several others had to be addressed regarding the actual surgery. Specifically, the anesthesia, the method of cranial opening, the method of securing the probe under the skull, the surgical personnel and the equipment required.

The anesthetic and anesthetic schedule were the typical ones used by AMRL/VS. The animal was preoperatively medicated with atropine sulfate (0.4mg/cc) and anesthetized with thiamyl sodium (Biotol 40mg/cc). Endotracheal intubation was established and the animal was maintained with 0.25% halothane in a mixture of 1:1 nitrous oxide:oxygen. The dog was placed in ventral recumbency and the skin of the dorsal cranium was aseptically prepared for surgery.

Two techniques were considered for making the cranial opening. The first was a full or partial craniotomy; that is removing all or at least a major portion of the animal's

cranium. This method would almost surely result in sacrificing the animal. A second drawback to that method was the limited amount of data that could be collected if the animal was sacrificed.

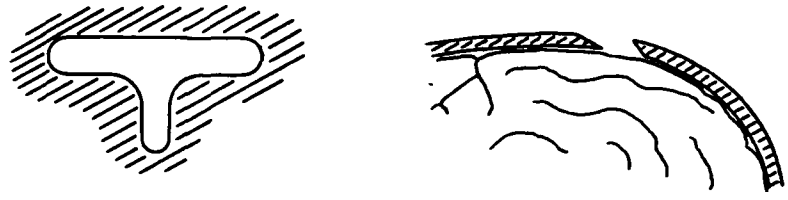
The second method considered was one of opening a window in the skull only large enough to accommodate the probe. Such a method would reduce the surgical complexity and increase the animal's chance for survival.

The latter was the method chosen, but with slight modifications. Discussions with doctors at AMRL/VS resulted in an agreement to attempt the implant by cutting a T-shaped opening in the skull above the occipital 1 region just to one side of the external sagittal crest. The implant would be completed by slipping the probe under the skull and meninges. Entering from the top (cross bar) of the T, the probe would be slid into position with the probe wires passing through the skull at the bottom of the T. Figure 5-5 depicts what would be the result of this procedure. As one can see, such an implant technique could result in considerable deformation of the cortex during probe implantation. Because this technique was developed specifically for this study and had not been tried or tested, further modifications during surgery were expected.

Once the probe was in place, insuring the probe remained stationary became a concern. If the probe were mobile, cortical damage due to abrasion would be likely.

FIGURE 5-5

"T" WINDOW; TOP AND SIDE VIEWS



Also, if the probe were not stationary, data collected from day to day would be difficult to compare.

A method frequently used by AMRL/VS for securing large cranial implants is described next. When preparing to close the wound, bone wax (Ethicon Inc. Somerville, N.J. #6515-00-965-2511) is packed into the window around the electrode wires. The bone around the window is roughed using a dental burr, and a short anchoring screw is screwed into the skull on either side of the window. A dental acrylic (Dental Acrylic Resin V-1000.3 & Orthocryl Liquid from Pronto IIxL Vernon-Benshoff) is prepared and spread over the bone wax, as well as around and over the anchoring screws. This method secures the implant and seals the wound. Except for the anchoring screws, the same method was employed for this implant.

The equipment and personnel required for the surgical procedure and follow-on testing are summarized below:

1. AMRL/VS facilities were used to perform the surgery and conduct all follow-on testing.

2. The Veterinary Sciences Division also provided the surgical team, technical advisor and life support equipment.

3. AFIT provided all system equipment outlined in Chapter IV. The engineering team consisted of the authors and their thesis advisor, Dr M. Kabrisky.

AFIT Probe

Following initial testing as outlined in Chapters II and IV, the probe had to be prepared for implanting. This preparation included removing the Molex connector and marking each of the nine wires for later identification. Once the connector was removed, the wires were inserted into a surgical elastic tubing with one end sealed up against the array backing plate and the other end plugged for added protection during the sterilization. Two types of sterilization were available, hot or cold. The autoclave (hot steam) method and the cold chemical wet bath (Sporicidin) were not used because both were suspected to be detrimental to the probe encapsulation. The method actual employed to sterilize the probe was a cold sterilization technique using the gas ethylene oxide. Time did not permit

testing the sterilized probe before implant. However, a test sample also sterilized by this technique showed no visually detectable degradation of either the polyimide encapsulant or the laquer coating on the wires.

Surgery

The left hemisphere was chosen as the location for the implant and when preparations were completed, surgery was undertaken. As planned, the anesthetic schedule presented above was followed and the entire operation lasted three and one-half hours. A major modification was made to the planned implant procedure. Although the window method was used and the initial opening was a T, the thickness of the probe dictated widening the T into a wedge and flaring the edges as shown in Figure 5-5. Once the probe was slipped under the skull, the membranes were lifted and the probe maneuvered under each side to place the probe in direct contact with the cortex. The probe and the tubing containing the wires were pulled back to the base of the opening. At this point bone wax was placed in the opening around the tubing, thereby preventing the probe from moving. After the skull was roughed with a dental burr, dental acrylic was spread over the roughed area, the bone wax and around the protruding surgical tube. The probe had been pulled back until the backing plate was against the inside of the skull in order to reduce the amount of pressure on the cortical surface. The tube and wires were then pulled subcutaneously and exposed at a point between the shoulder

blades. A loop was left in the length of tubing from the skull to the shoulders to allow for normal motion and reduce the amount of tension at the point where the tubing entered the skull. The wound was then sutured leaving only surgical tubing containing the nine small wires emerging from between the shoulders. The Molex connector was replaced and the tubing sutured to the skin. A jacket was put on "Ricky" which protected the connector while allowing easy access to it at the daily testing sessions.

As already mentioned, the life of the probe was not known specifically though a minimum of three days was expected. However, attention was now focused on how well "Ricky" would tolerate the implant. Pressure on the cortex induced by the probe could result in edema or necrosis of the tissue under the probe, either of which would limit data collection and endanger Ricky. More importantly, the fear of infection was ever present. In an effort to control both edema and infection, Ricky was given injections of steroids and antibiotics (cloromycetin).

Ricky survived the surgery and the antibiotic apparently controlled infection and edema in the brain. The probe survived and functioned seventeen days. Data were collected over this seventeen day period.

On the seventeenth test day, it was noted that the wound above the implant area was partially open and oozing a clear fluid. Inspection of the wound and fluid led to the theory that an infection had progressed up the surgical tubing from the shoulders where the tubing emerged. There

was growing concern as to whether or not the infection had or would soon enter the brain. In an effort to save both Ricky and the probe, removal surgery was scheduled for two days later, the nineteenth day after implant.

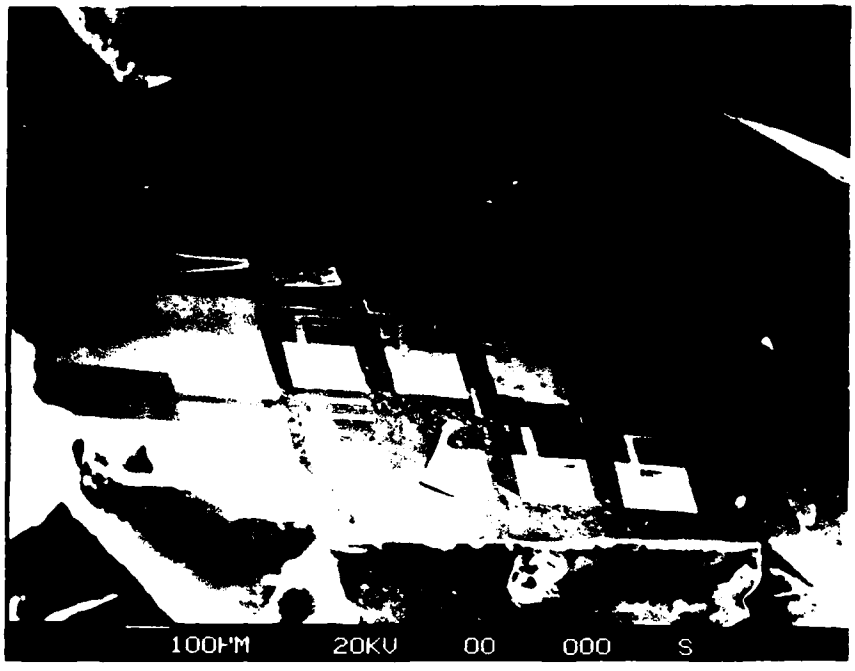
After removal, the probe was examined. Electron microscope pictures, included as Figure 5-6, show obvious damage to the array itself. The damage may have been the result of being in the CSF or a result of the removal process.

The nature of the damage and the fact that data was recorded up to the seventeenth day strongly suggested the damage to be a result of probe extraction. Time did not permit thorough analysis of the probe and although the probe was damaged, the cortex area under the probe appeared normal. That is to say there was no tissue necrosis nor edema. Ricky was alive and the probe was still intact though somewhat damaged.

FIGURE 5-6a

AFIT MULTIELECTRODE ARRAY PROBE ASSEMBLY
AFTER EXTRACTION; ARRAY CLOSE-UP

(Photographs taken by Scanning Electron Microscope



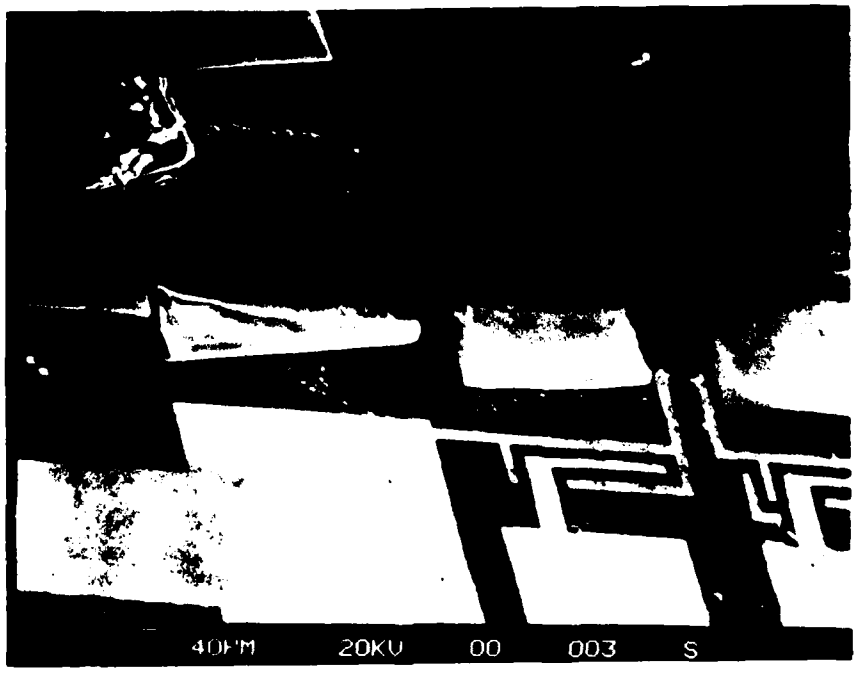
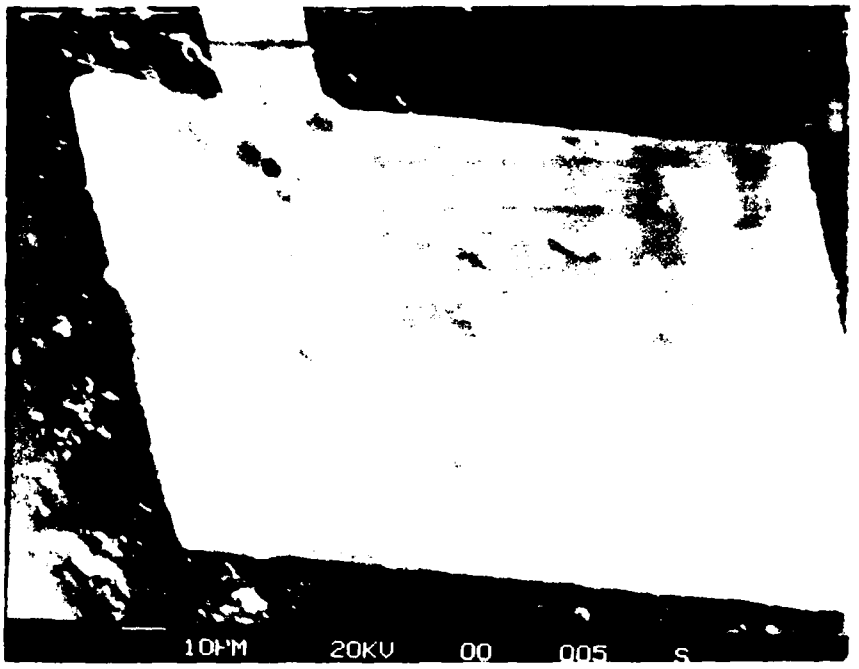


FIGURE 5-6b

AFIT MULTIELECTRODE ARRAY PROBE ASSEMBLY
AFTER EXTRACTION; SENSING PAD CLOSE-UP

Photographs taken by Scanning Electron Microscope



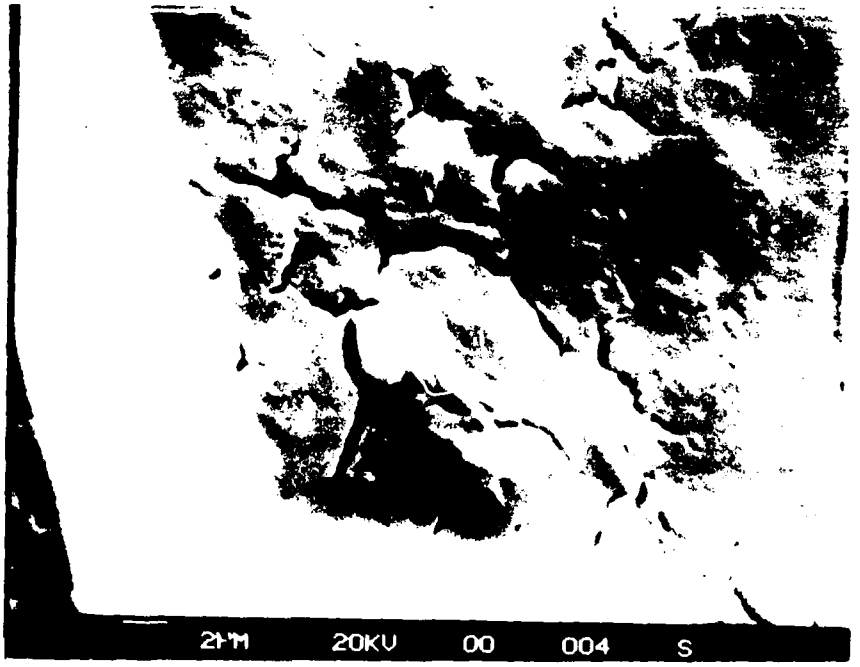
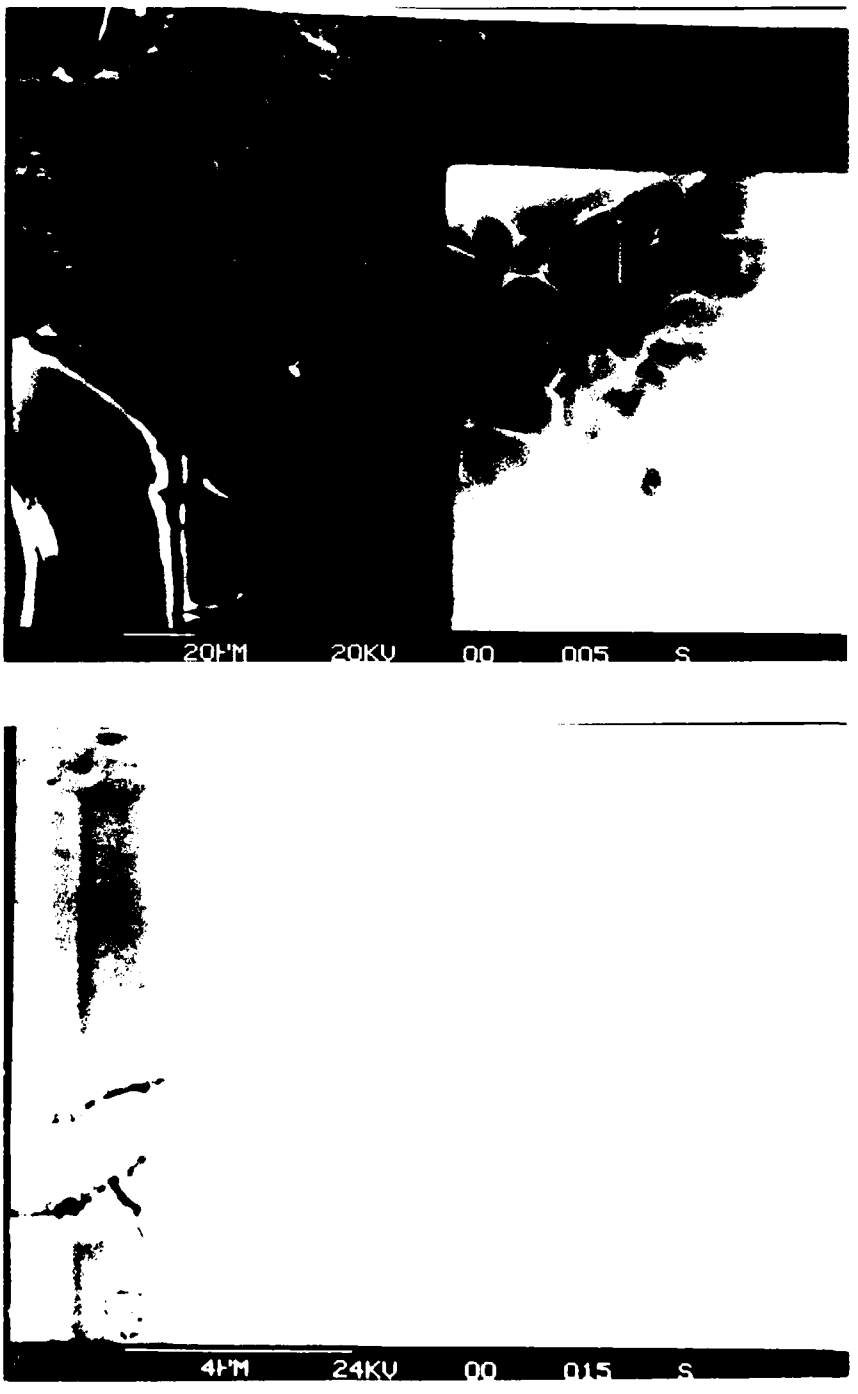


FIGURE 5-6c

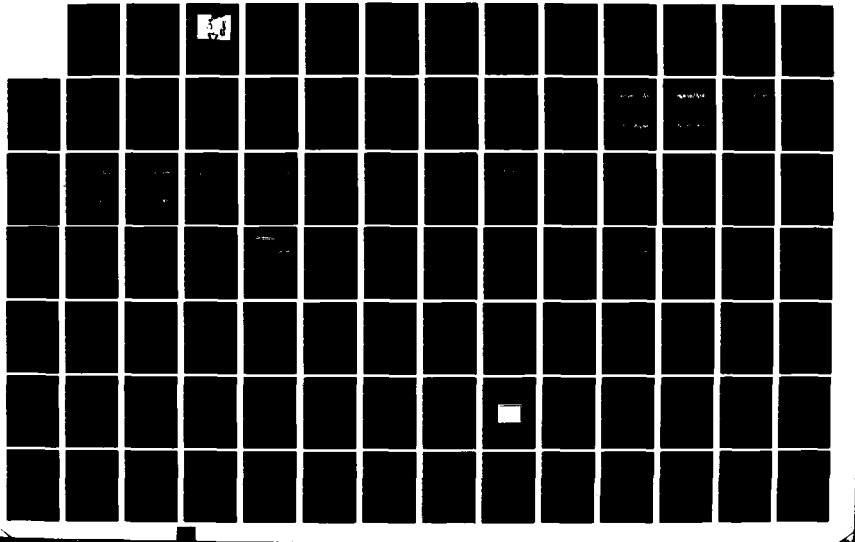
AFIT MULTIELECTRODE ARRAY PROBE ASSEMBLY
AFTER EXTRACTION; FOREIGN SUBSTANCE CLOSE-UP

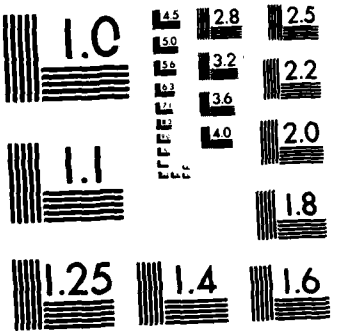
Micrographs taken by Scanning Electron Microscope



AD-A124 878 THE FIRST CORTICAL IMPLANT OF A SEMICONDUCTOR MULTIELECTRODE ARRAY: ELECT..(U) AIR FORCE INST OF TECH WRIGHT-PATTERSON AFB OH SCHOOL OF ENGI.. 2/3

UNCLASSIFIED R W HENSLEY ET AL. DEC 82 AFIT/GE/EE/82D-29 F/G 6/16 NL





CHAPTER VI

DATA COLLECTION

Introduction

During the course of the experiment, the authors were concerned with two types of data. First, physiological data, that is Ricky's condition, and second, cortical bioelectrical data collected from the probe. This chapter is divided into two areas, one discussing the collection of physiological data and the other discussing the collection of cortical bioelectrical data.

DATA

Physiological

From the outset, Ricky (Figure 6-1) seemed to be unusually agreeable and contented. He showed no outward signs of discomfort and never in any way acted agressively. His disposition throughout the experiment was pleasant and his "good-nature" came to be identified by what the authors refer to as the "tail wag response". Even while under anesthesia, he would respond to his name with a tail wag. In all respects, he exhibited "normal" behavior for a laboratory animal. He ate well, maintained normal body temperature and showed no signs of complications as a result of the surgery. Additionally, his visual fields appeared undamaged. He exhibited normal pupil response and could easily track an object with his eyes.

FIGURE 6-1

EXPERIMENTAL SUBJECT; "Ricky"

Brain Activity

At first, data from the probe was collected daily because the life of the probe was suspect. Daily data collection permitted monitoring of both Ricky and the probe. Data collection continued for twelve consecutive days. Since the probe showed no signs of failure and Ricky was healthy, data collection was reduced to every other day. Referring to Chapter III, recall that the drive circuitry had been designed to enable data collection in either an absolute or a differential mode. For the first several days, data was collected in the differential mode only. The remainder of the data collection was done in both modes.

Data Analysis

As previously mentioned, the exact nature of the data to be derived from this new electrode and research technique could only be speculated upon. However, in the beginning, a signal similar to conventional clinical EEG was certainly expected. Based on initial data analysis, this suspicion was confirmed. Time constraints precluded complete data reduction and analysis. Appendix A contains some of the reduced, digitized data and associated strobe signals. It is obvious that the data are very similar to scalp electrode EEG (Ref. 19) and therefore, is considered to be EEG, but at a high, perhaps ultimate spatial resolution. Atypically for EEG signals, the data presented in Appendix A show that at least some of the signals are to be on the order of several hundred microvolts. Though an absolute statement cannot be made at this time, the fact that the data consistently shows a base frequency of five to eight cycles-per-second (i.e. exactly the frequency range of canine scalp EEG) supports the theory that these data are not artifactual nor electrode noise (Ref. 18:365-366). Correlation analysis of the signals sampled from adjacent electrodes remains to be accomplished.

In an attempt to confirm the nature of the data, a strobe was implemented to stimulate the subject. Data collected would then be analyzed for the presence of an evoked response. Initial analysis did not show any evoked response. The initial reaction to this result was that an

evoked response might not be present at the fine spatial level being examined. Thus, for verification of the presence of an evoked response, an indifferent electrode was added (on the ear) and measured with respect to the reference plane on the array. Data collected from the additional electrode appeared to show an evoked response (see Appendix A). Further analysis also revealed the possible presence of an evoked response in the signals sampled by the array. However, if an evoked response is present at this spatial resolution, it has a slightly different form. Time constraints prevented detailed analysis of the data collected and more analysis is required before definite conclusions can be drawn.

CHAPTER VII

CONCLUSIONS

AFIT PROBE PROCESSING

Detailed post implant examination of the AFIT Probe showed no serious deterioration of the polyimide encapsulating material. Although the polyimide seems to have absorbed some body fluids (essentially water), it protected the AFIT Array. Therefore, it can be concluded that polyimide is a workable, readily processed, substance suitable for use as an encapsulant.

However, no statement can be made concerning a "best" encapsulant. German also recommended phosphosilicate glass (PSG) which has yet not been evaluated as an encapsulant (Ref. 7:29). Furthermore, other materials besides polyimide and PSG could very well be more suited as an encapsulant.

Chip Size

After surgical implant and removal, it was quite apparent that the final size of the probe must be smaller. In general, the size of the final probe must be related to the cortical curvature of the experimental subject. The final probe should be sufficiently small, relative to the curvature of the cortical sheet, to prevent significant displacement the cortex.

The probe used for this implant was one centimeter square. Even though there was no apparent edema or necrosis, the probe was somewhat large for a dog's skull.

Also, the square corners of the backplate supporting the AFIT array caused implant and removal problems. It is obvious that the backplate should be circular and smaller.

HARDWARE

External Drive Circuit

The external drive circuitry worked well, thereby proving the design methodology. The independent system operation capability aided greatly in testing the entire experimental system prior to implant.

It can be concluded that the system signal to noise ratio is good. Even in the presence of occasional ground loops, noise did not effect the output signals. However, each device in the system must be examined channel by channel to determine the noise levels present.

DATA

Physiological

It may be concluded that this technique is a viable method of chronic cortical research. The test subject ("Ricky") survived both implant and removal of the probe without any detectable after effects. In fact, Ricky is presently alive, well and functioning as a "normal" dog. Ricky responds normally to visual stimuli in both visual fields.

Analytical

After removal of the AFIT Probe, the Air Force Avionics Laboratory conducted an inspection of the probe using an

electron microscope. The surface of the probe, particularly in the area of the multielectrode array, was scanned to determine the probe's condition. The scans revealed two problems; metal-to-silicon adhesion and a foreign substance (Ref. 24:9).

The metalization layer of the AFIT array consists of chrome, platinum and gold. Figure 5-6 shows there was obvious metal delamination. Whether the adhesion problem is the result of the chrome-silicon boundary or the combination of metals is unknown. Further research in this area is under way.

The presence of a foreign substance on the surface of the probe was a most unexpected discovery. When the probe was first removed, initial visual inspection revealed an intact probe. Later, after several cleanings, the electron microscope revealed a thin layer of a partially opaque substance over the entire surface of the probe. Significant consideration should be given to analysis of the probe before and after sterilization and implant.

Analysis of the JFET's led to the conclusion that JFET parameters were not optimum. Leakage from gate to drain causes a DC offset in the signal stream. Further, the pinch-off voltage does not pinch-off current flow at the specified voltage. These are minor but obvious flaws in the JFET's.

COLLECTED INFORMATION

Only a brief preliminary analysis of the collected data was performed. Nevertheless, it can be concluded that the data collected is EEG. Furthermore, there is evidence of VER between essentially adjacent BCE's, though further analysis is required to confirm this.

SUMMARY

This research effort has proven the AFIT Multielectrode Array can be a valid cortical research tool. In addition, it appears that the AFIT array can be a chronic implant. The AFIT array should open a new era of cortical research.

CHAPTER VIII

RECOMMENDATIONS

AFIT ARRAY MODIFICATIONS

The major problem confronting the AFIT Multielectrode Array is sodium contamination. Considerable research into encapsulation techniques and materials has led to a successful implant. However, there should be much more research and development in the area of "sodium hardening". That is, designing into the integrated circuit and/or the JFET's themselves a certain sodium tolerance. While the JFET source pad, that is the array sensing electrode, must come in contact with the cortex, the remainder of each JFET must be protected.

At present the array configuration is such that each JFET is built adjacent to the sensing pad. Research should be conducted in the area of manufacturing an array of sensing pads with associated JFET's in a "remote" region of the chip. Additionally, further research in JFET technology is warranted. This particular study was accomplished using an array designed and fabricated by the technological standards of five years ago. Since the original devices were manufactured most of the continued work has been in the realm of accomplishing an implant and little has been done to improve or change the array design and fabrication.

Reference Plane

In the present configuration of the AFIT array as shown in Figure 3-1, there is an L-shaped reference electrode. It was originally intended as a two dimensional reference for absolute voltage measurement. If, however, BCE's exist (i.e. independent voltage generators) as hypothesized, linear approximation is not a valid method of analysis. Further, the L requires the data analyst to make a two dimensional linear approximation, which is not necessarily valid.

It would be most advantageous to reduce the reference electrode to a simple bar on only one of the four sides of the JFET array. This action would reduce the absolute voltage measurement problem to that of simple linear analysis, if possible. Such a change would aid significantly in data reduction/analysis and in defining the exact size of a BCE. However, the ability to differentially measure the voltage between JFET's may render the reference electrode unnecessary. Finally, the addition of multiplex circuitry to the chip (see Appendix F) or an increase in the size of the array will certainly require access to the array from several directions. Reducing the reference electrode would facilitate the most certain "growth" of the AFIT array.

Bonding Pads

Although the AFIT array is very small (1000 x 1000 microns), the entire chip is much larger (1 centimeter square) (see Figure 2-2). Large bonding pads are located

along the outside edges of the chip to facilitate interface of the chip to the "outside world". The bonding pads are intentionally large; meant to provide adequate space for wire leads (i.e. 28-30 AWG) (Ref. 5:70).

By the time the chip is passivated and encapsulated, the resulting probe is almost prohibitively large. It is much more desirable to reduce the size of the probe such that it could be implanted through a hole. (drilling a "large" hole (i.e. one half inch diameter) in the skull is not uncommon.)

Size reduction of the AFIT chip has been accomplished by removing the bonding pads. The remaining chip is much smaller (1500 microns on a side). However, interface to the outside world becomes more difficult. It is possible, however, to attach connecting wires to appropriate points of the metalization pattern prior to encapsulation using silver contact paint. The resulting probe should be between one-fourth and three-eighths inch in diameter.

Packaging

It is also desirable to reduce the depth (i.e. thickness) of the probe. The current process uses epoxy glue as the final encapsulant. The epoxy retains the connecting wires and provides a rigid backing for the chip. The layer of epoxy applied was not thin due to the viscosity of the epoxy, therefore the finished probe was rather thick. It was also noted during testing that the epoxy tended to absorbed some of the solution in which it was emersed. It

is recommended that a new material be sought which does not absorb fluids yet permits thinning prior to application. Every effort should be made to minimize the thickness of the probe.

The shape of the probe is also very important. During probe implant and removal, it was obvious that the probe's pointed corners were undesirable. The corners caught in the tissue (i.e. dura) during implant and removal. A circular shape is preferable and because the probe's shape is determined by the backing (or support) plate a circular backing plate could easily be incorporated. The result would be a probe with no sharp edges or corners. Also, a small circular disc would slide between layers of tissue more easily.

Connecting Wires

Wires which attach to the chip were bent around the edge of the backing plate and gathered into a bundle in the back. This configuration is, at best difficult to maintain while encapsulating the chip. Holes may be "laser-drilled" through the backing plate thus permitting the chip connecting wires to pass directly through. This technique also serves to secure the chips position on the backing plate while reducing the perimeter thickness of the probe.

A NEW GENERATION AFIT ARRAY

Since AFIT now has a rather small supply of (Fitzgerald fabricated) multielectrode arrays, it is apparent that new devices must be fabricated. The new devices should actually

be a new generation AFIT Multielectrode Array incorporating at least the following recommendations.

First, array size should be increased to 16 x 16. This array size would not significantly increase the size of the chip but would certainly provide more representative data for analysis.

Second, an on-chip multiplex circuit should be distributed across the space available between the "sensing" electrodes. Normally, engineers tend to think in terms of functional blocks and when implemented, the functional blocks often become discrete physical blocks. Such is the case of a multiplexer design in Appendix B where the AFIT array is physically separated from the multiplexing function as requested by the authors. It is possible and efficient to logically distribute the the multiplexing function across the surface of the AFIT array.

Multiplexers are essentially binary counters and decoders. Both the counters and decoders should be logically distributed through the AFIT array. "Logically", implies that binary order is observed. Distributed across row one of the array would be that part of the decoder necessary to switch the elements of row one . The same being true for subsequent rows.

Third, VDD to VSS design parameters for the AFIT array and multiplexer should be reduced to six volts. The present AFIT array is being operated at a six volt difference with no apparent difference in JFET characteristics.

Furthermore, the multiplexer of Appendix F was designed to operate at +6 to -6 volts. If possible, a further reduction of the supply voltages could also reduce any noise which the multiplex circuitry may generate.

Finally, a connection should be provided from the "sensing pads" to the external drive circuitry. Access to the JFET sources would permit the external drive circuitry to inject a test signal into the JFET's which may be compared to the output signal. Present methods of testing use either a neeedle probe which may scratch the contact pads or a saline bath which contaminates the surface; either method potentially renders the probe unusable for implant. Access to the JFET sources would permit non-destructive testing of AFIT arrays before implant.

HARDWARE

Dark Field Mask

The procedure for the final chip encapsulation was developed using a light field mask and therefore, negative photoresist. Polyimide in a partially cured state is also etched by positive photoresist developer; so another technique using a dark field mask might produce better results than those obtained with the light field mask. This matter warrants some study.

Probe Conductors

Nine very small (35 AWG were used) wires carry signals to and from the AFIT array. They exist between connector J4 and the chip. Although very small, these wires must be

flexible. In addition, the wires must be insulated with a non-toxic material. Thirty five gauge transformer wire was used for this thesis effort. However, it was easily "kinked" and broken. Other wire, suited to this purpose, should be sought. (A surgical supply company could be a source.)

Probe Connector J4

The probe connector J4 should be of the zero connecting force variety. Such connectors are usually known by the generic term "Cannon Plug". A threaded portion of these connectors supplies the force necessary to make or break electrical contact. If this type of connector is not used, the jerking motion required to separate the receptacle and plug may damage the small wires, the connections at J4 or the animal's wound at the entry point. And as previously mentioned, such an infection could proceed through the corridor provided by the wire bundle to the implant site.

Microprocessor External Drive Circuit

Each new development effecting the AFIT array usually results in a subsequent modification of the external drive circuitry. Consequently, the external drive circuitry presented herein is a third generation circuit. Until now, there was no evidence that the AFIT array really worked as designed, and therefore, there was no proven external drive circuitry. However, as a result of this study, the technique for driving and isolating the AFIT JFET's has been proven. Any future design should allow the external drive

circuitry to be expandable, flexible, reliable and capable of testing AFIT arrays. A relatively simple microprocessor system should be used in the design of a next generation external drive circuit.

Microprocessors are very reliable, compact, expandable and flexible. In fact, with a micro-processor based drive circuit, additional operating features could probably be accomplished by simple changes in software/firmware. Additionally, the design should be accomplished using CMOS technology as CMOS and JFET characteristics are similar (ie. +VDD to -VSS supply voltages). The micro-processor interface to the AFIT array should be a Peripheral Interface Adapter (PIA). A PIA would provide the computer with 8 or 16 very high speed digital input/output lines (i.e. necessary for increasing the array size). And the addition of a Digital to Analog Converter (DAC) and an Analog to Digital Converter (ADC) to the circuit would permit the creation and sampling of time-varying waveforms which may be used to check the operation of the AFIT array.

METHODOLOGY

Implant

Although further refinement of the AFIT array is certain, the present array could be used to determine the exact size of a Basic Computational Element (BCE). A stereotaxic machine could be used to translate and rotate the probe across the surface of the cortex; some machines are capable of movement on the order of microns. Such

minute movement is sufficient to determine the width, shape and relative spacing of a BCE.

However, the next implant should concentrate on collecting data which may, under analysis, suggest the type of process that exists between "primary" and "associative" cortex. This would, of course, require the use of at least two AFIT arrays (one on primary visual and one on associative visual cortex) and a well planned experimental method which should include the possiblity of using the AFIT array to stimulate primary visual cortex and observe the results in associative visual cortex. Initial implant of only one AFIT array prohibited verification of this procedure. Recall, however, that JFET's were desirable because they are essentially two-way switches and permit insertion of data into the brain just as easily as they allow it to be collected.

SURGERY

A more simple surgical technique should be investigated. One such technique would be to bore a hole in the test subject's skull. With a smaller probe, boring a hole may be a more suited technique for future experiments.

The hole should be filled with bone wax and dental acrylic after the probe is positioned and the membranes are closed. The bone wax should follow the contour of the interior skull and not penetrate into the dura. On the outside, bone wax should not fill the hole; space must be available in the hole to permit dental acrylic to secure the

probe.

Where dental acrylic meets the probe wires, there cannot be any sharp edges which may cut into the wires. Cured dental acrylic has a tendency to develop sharp edges unless caution is exercised during application. In addition, the cure temperature can be very high and might damage the underlying tissue. A method of dissipating this heat should be investegated.

A small skull "gromet" is recommended to prevent any sharp edges of the dental acrylic from rubbing against the wires. The gromet should have an hour-glass shape with a hole in the center through which the wires pass. The ends must be smooth around the edge. One end of the gromet should be secured to the array backplate during encapsulation. The other, must rise slightly above the dental acrylic (on the outside of the skull) after implant. In this manner, the dental acrylic will secure the gromet and subsequently the probe yet, never touch the wires.

DATA COLLECTION AND ANALYSIS

One of the many data to be evaluated after an experiment is the condition of the probe itself. For comparison this requires a critical evaluation of the probe both before and after the experiment. The recommended method of accomplishing such an evaluation requires the use of an electron microscope to take detailed photographs of the probe before and after sterilization and implant. Members of the Device Technology Group within the Microelectronics

Branch of the Air Force Avionics Laboratory have been most cooperative in providing such services for the study of the AFIT array.

Another data is the signals extracted from the cortex. Analysis of this data is a rigorous process and requires an in-depth knowledge of electroencephalographic signals. Therefore, it is highly recommended that the researcher who endeavors to analize the cortical data be familiar with EEG signal forms, types and meanings.

From all information collected, this research noted that the EEG signals taken during periods when the animal was anesthetized differed somewhat from those taken during periods of normal activity. However, at this time there is, insufficient "anesthetized" data to suggest that anesthetics have significant effects upon the results of experimentation performed during anesthetized periods. Much more data should be taken while the animal is anesthetized for comparison with "unanesthesized" data.

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APPENDIX A

The material contained in this appendix is a sample of the data collected during the time of the implant. To include plots of all the data is neither practical nor necessary. The plots presented herein are a representative sample of the data analyzed. The abscissa of each plot is labeled in volts and the ordinate is labeled as points from a computer data file block. The plot routine used scales the data to be plotted so that the plot field is essentially full; thus the scale on any two plots may differ. Futhermore, the data recorded had been significantly amplified. Nonetheless, although not evident here, all data ranged from one-half to one millivolt peak to peak. (Unless otherwise noted 511 points equals four seconds of data.)

Software implemented to analize evoked response is presented in Appendix G. All other software used to reduce the collected data is on file at the Air Force Institute of Technology, Signal Processing Laboratory. This includes the programs DIGITIZE, CNVRT, PLOT AND CAT (Ref. 25).

Figures G-1 through G-10a represent data taken differentially between two column sensing pads on a single row of the AFIT array. Each figure label gives the columns between which the differential was calculated, the row, the test day and the computer blocks where the data was stored.

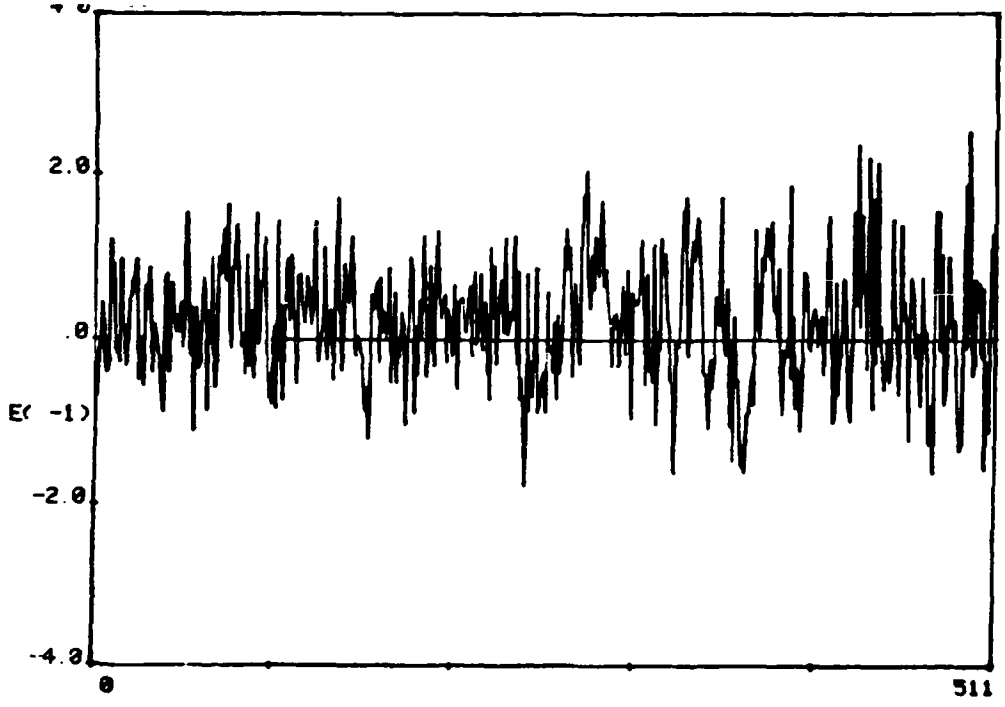


Figure G-1a: Columns 1 and 2; Row 2; Day 5; Blocks 6-9

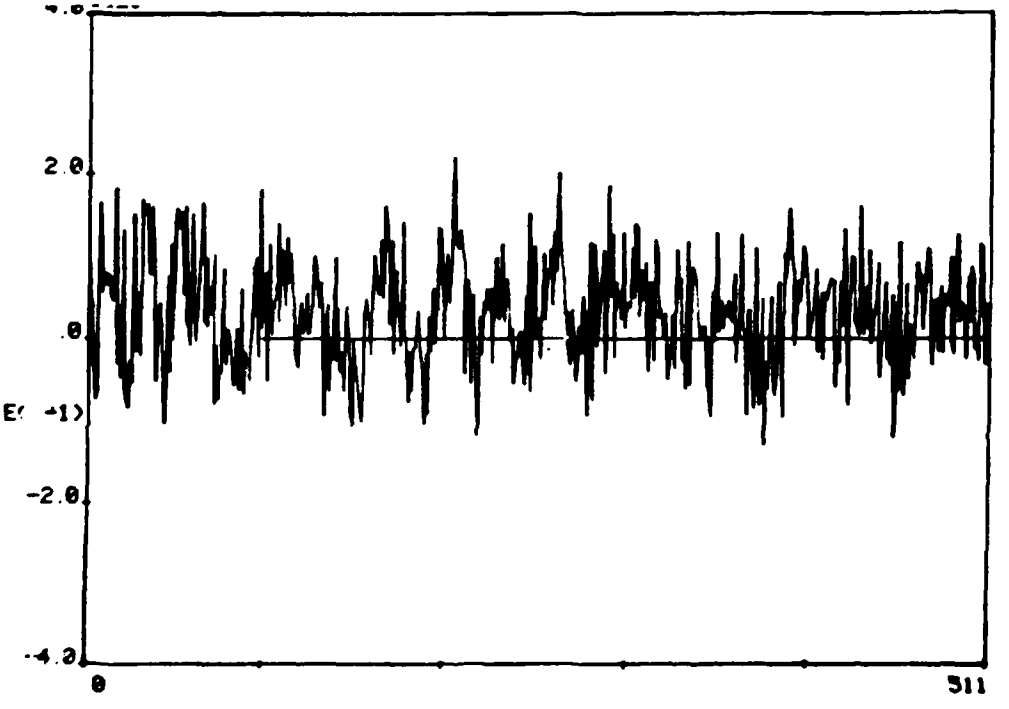


Figure G-1b: Columns 1 and 2; Row 2; Day 5; Blocks 10-13

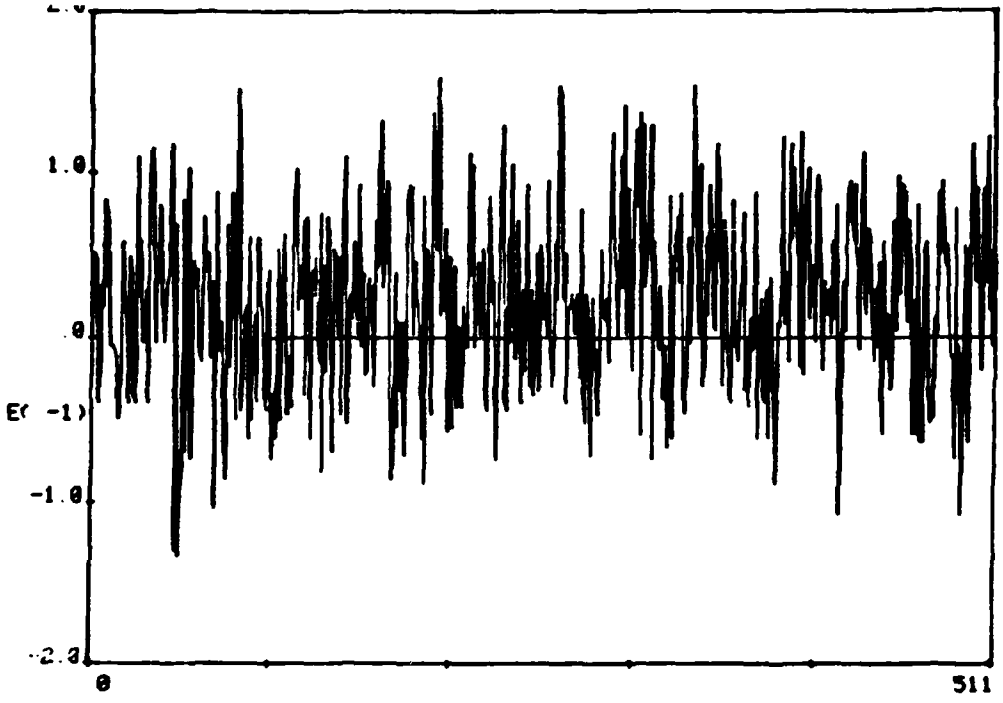


Figure G-1c: Columns 1 and 2; Row 2; Day 5; Blocks 14-17

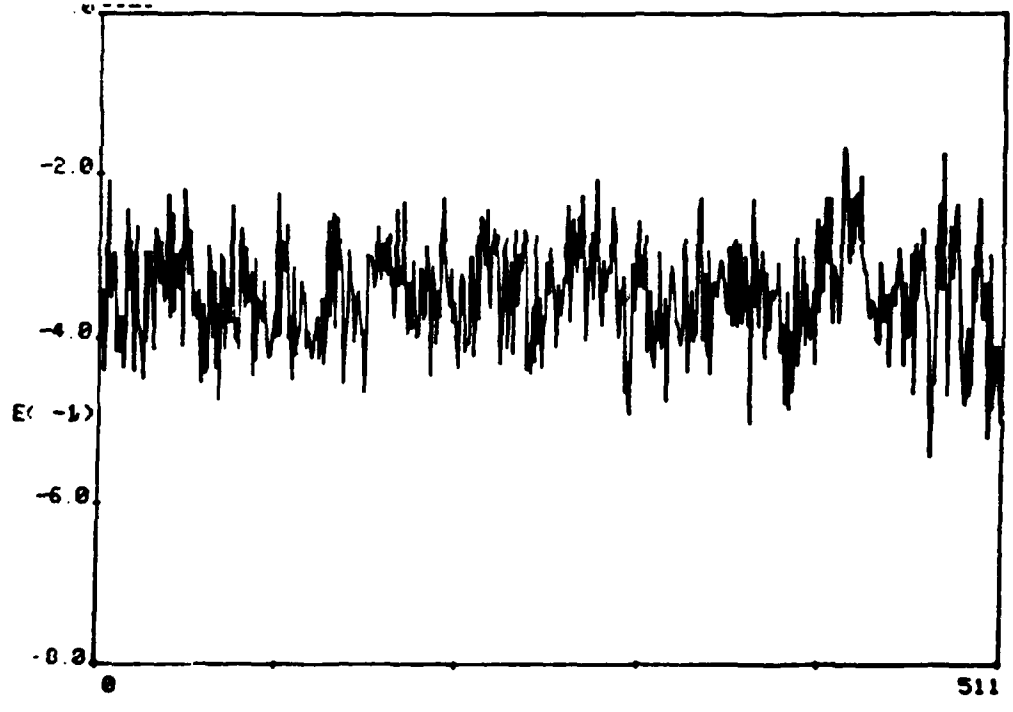


Figure G-2a: Columns 1 and 2; Row 3; Day 5; Blocks 5-8

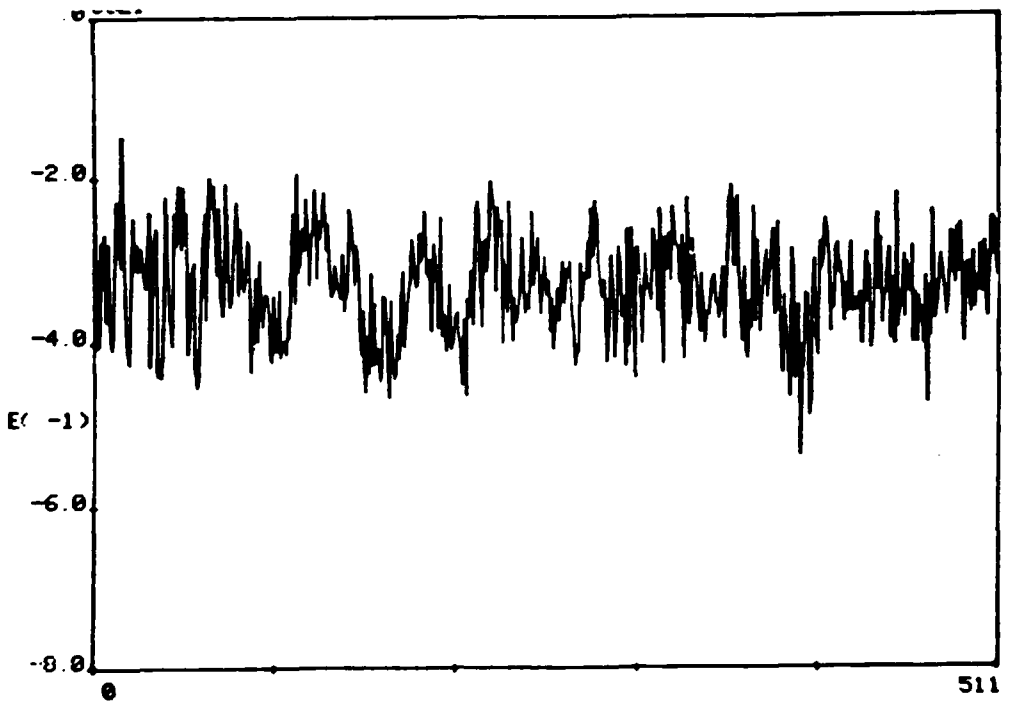


Figure G-2b: Columns 1 and 2; Row 3; Day 5; Blocks 9-12

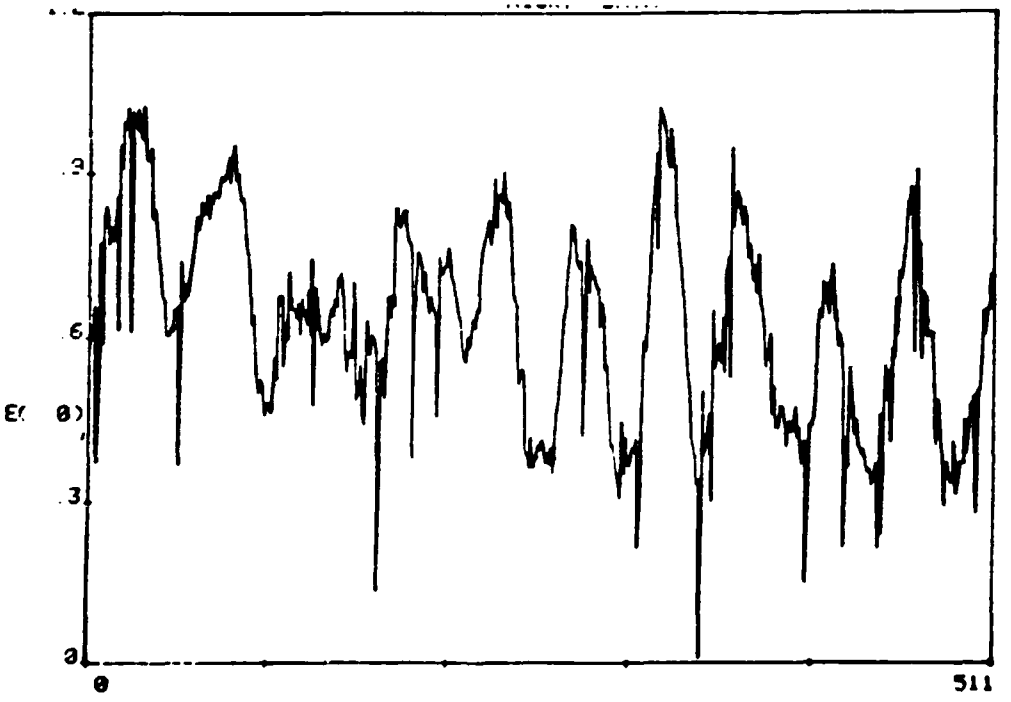


Figure G-3a: Columns 1 and 2; Row 2; Day 3; Blocks 1-4

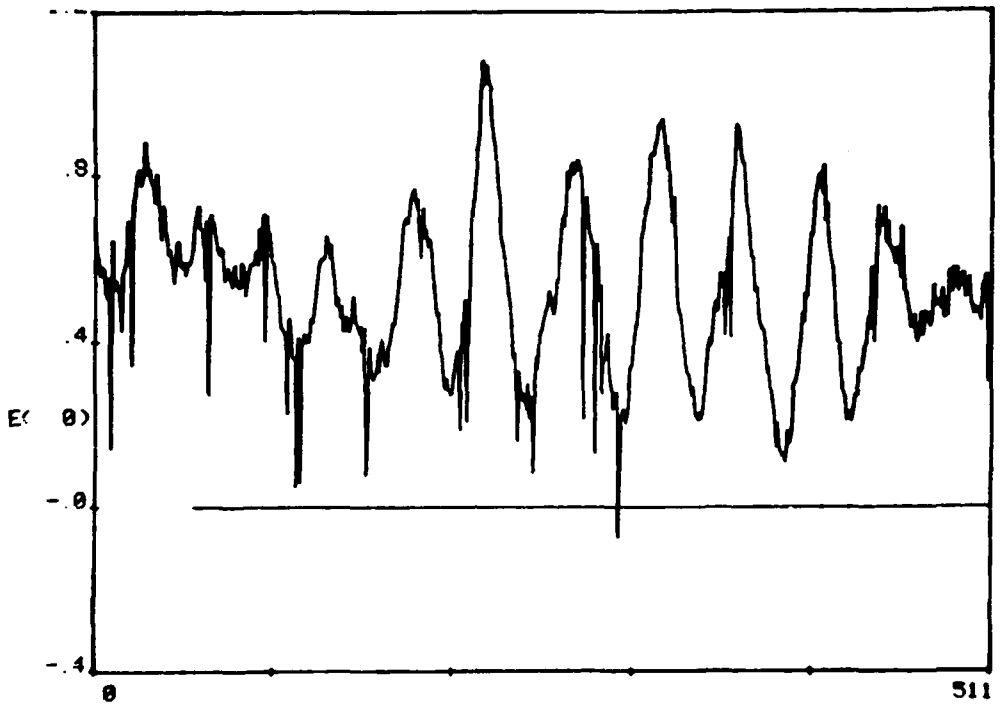


Figure G-3b: Columns 1 and 2; Row 2; Day 3; Blocks 18-21

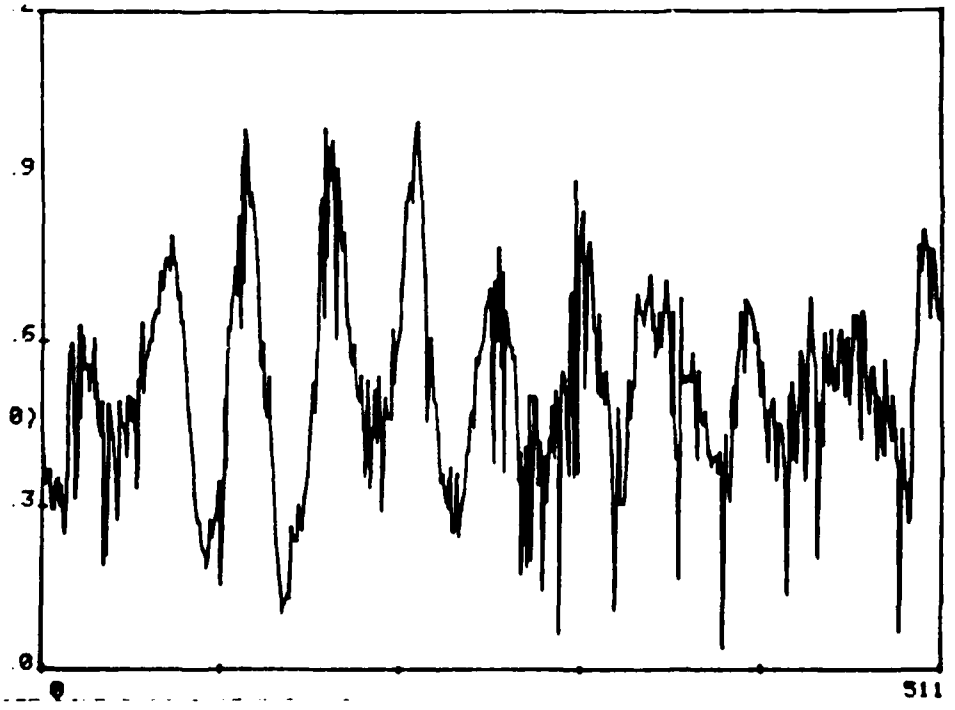


Figure G-3c: Columns 1 and 2; Row 2; Day 3; Blocks 22-25

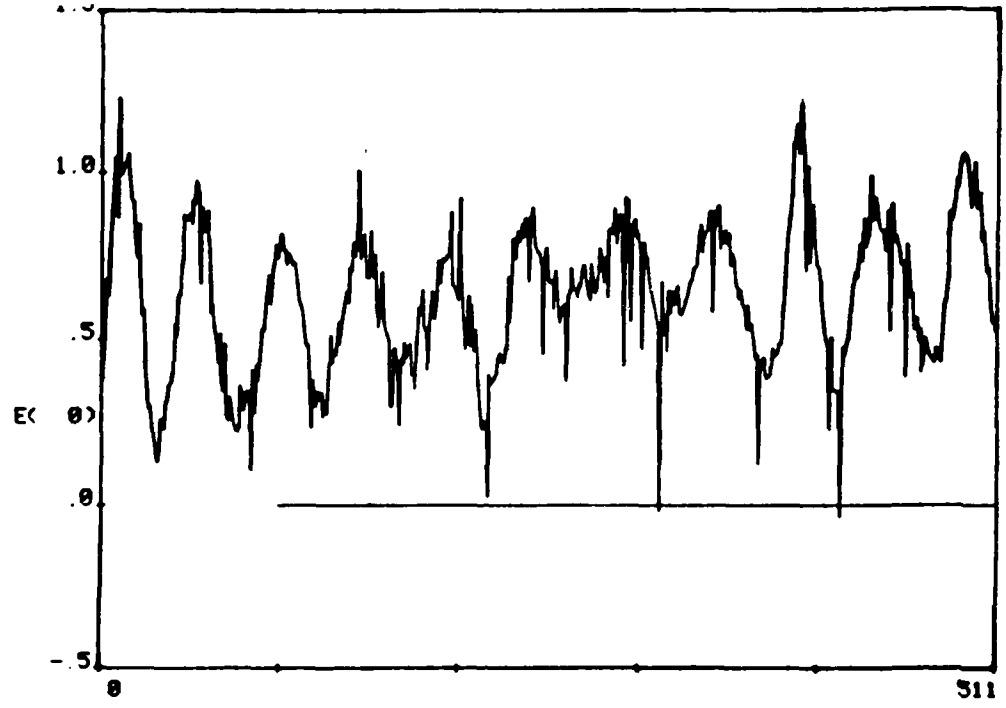


Figure G-3d: Columns 1 and 2; Row 2; Day 3; Blocks 65-68

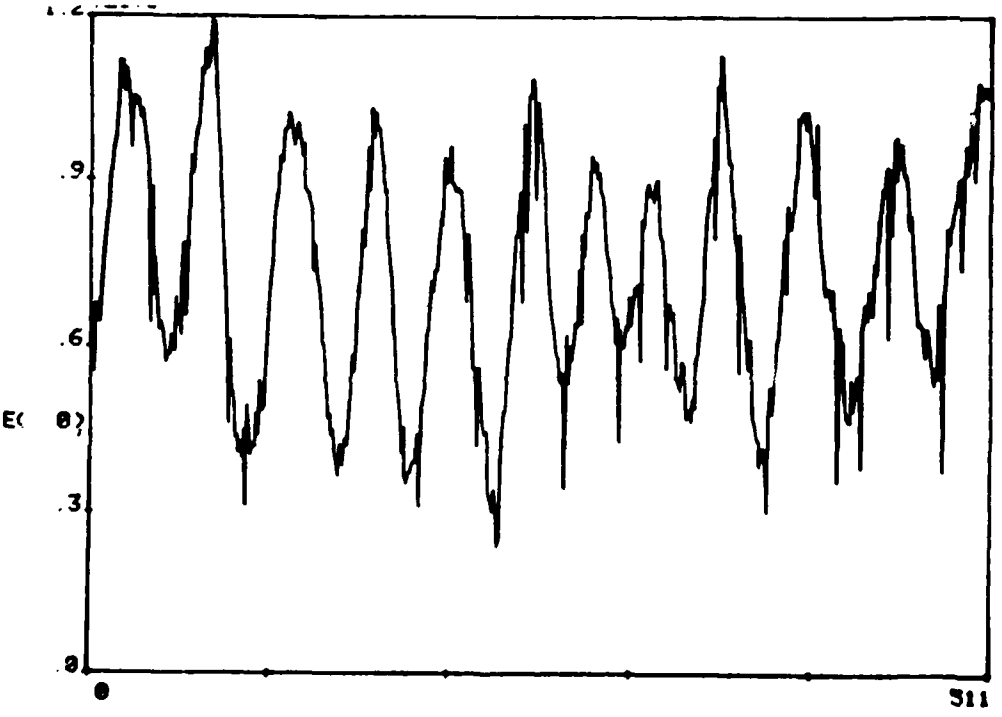


Figure G-3e: Columns 1 and 2; Row 2; Day 3; Blocks 69-72

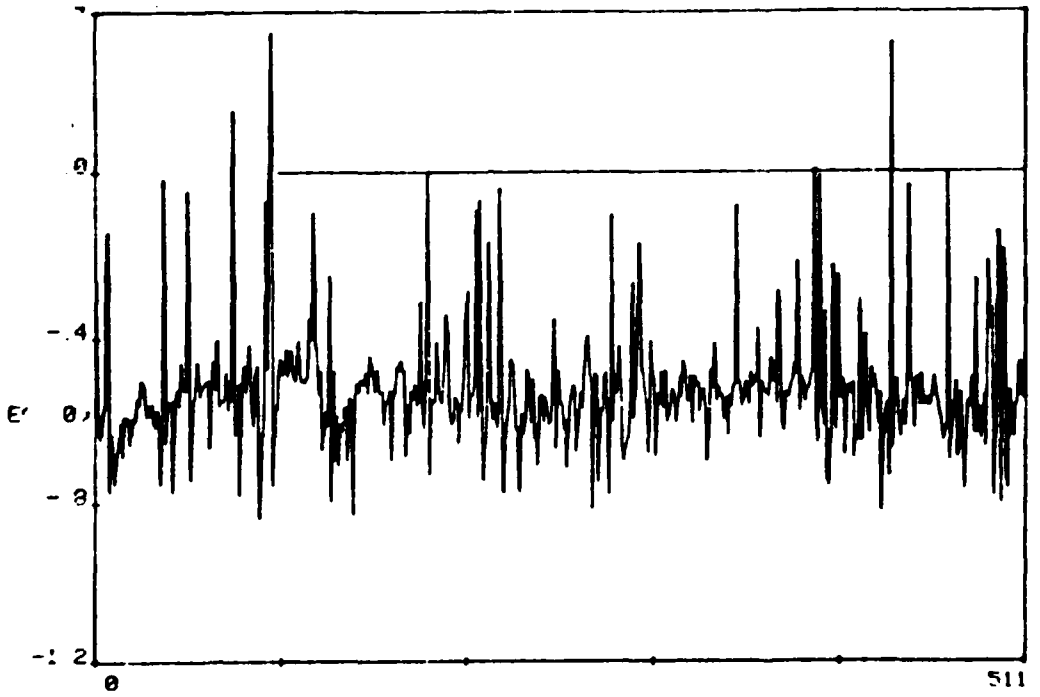


Figure G-4a: Columns 2 and 3; Row 4; Day 10; Blocks 5-8

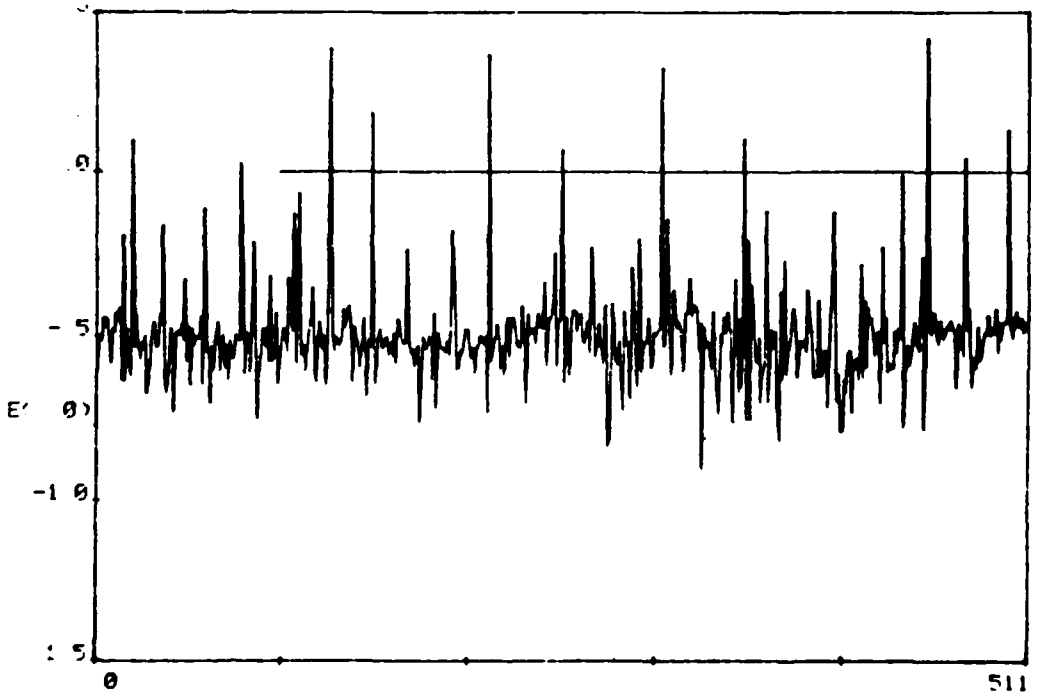


Figure G-4b: Columns 2 and 3; Row 4; Day 10; Blocks 9-12

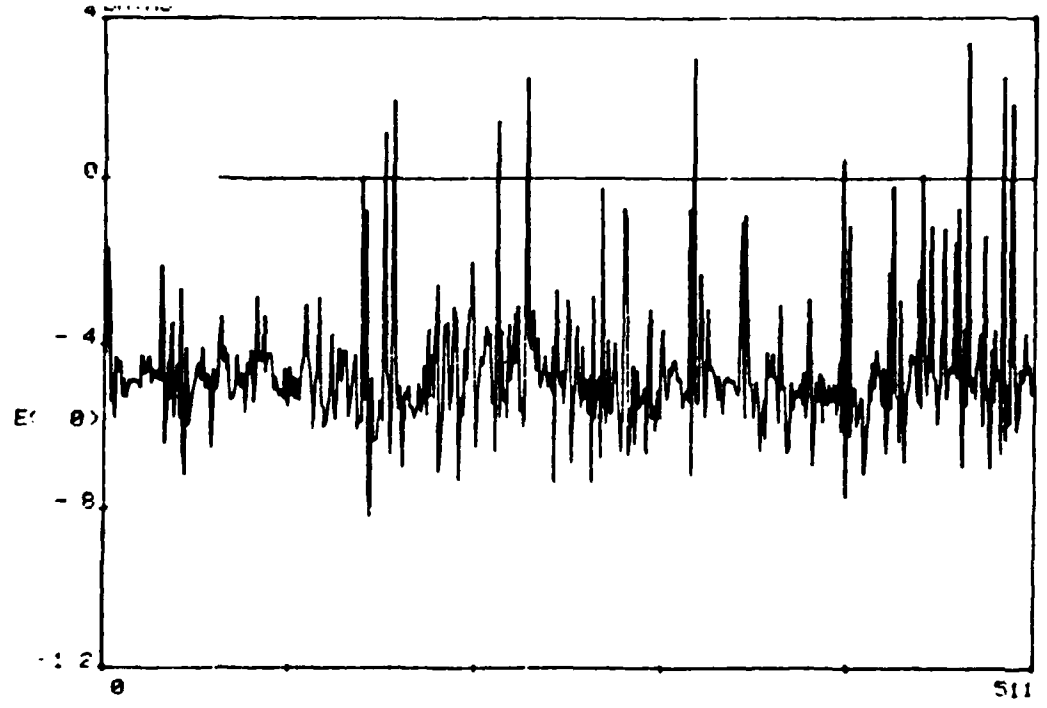


Figure G-4c: Columns 2 and 3; Row 4; Day 10; Blocks 13-16

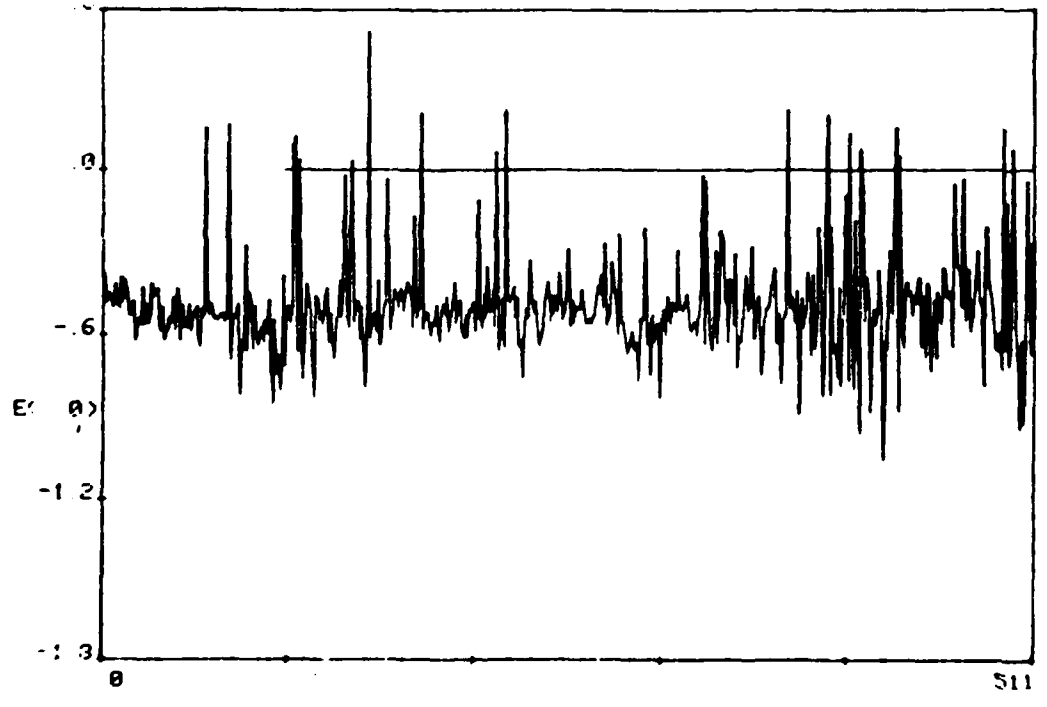


Figure G-4d: Columns 2 and 3; Row 4; Day 10; Blocks 17-20

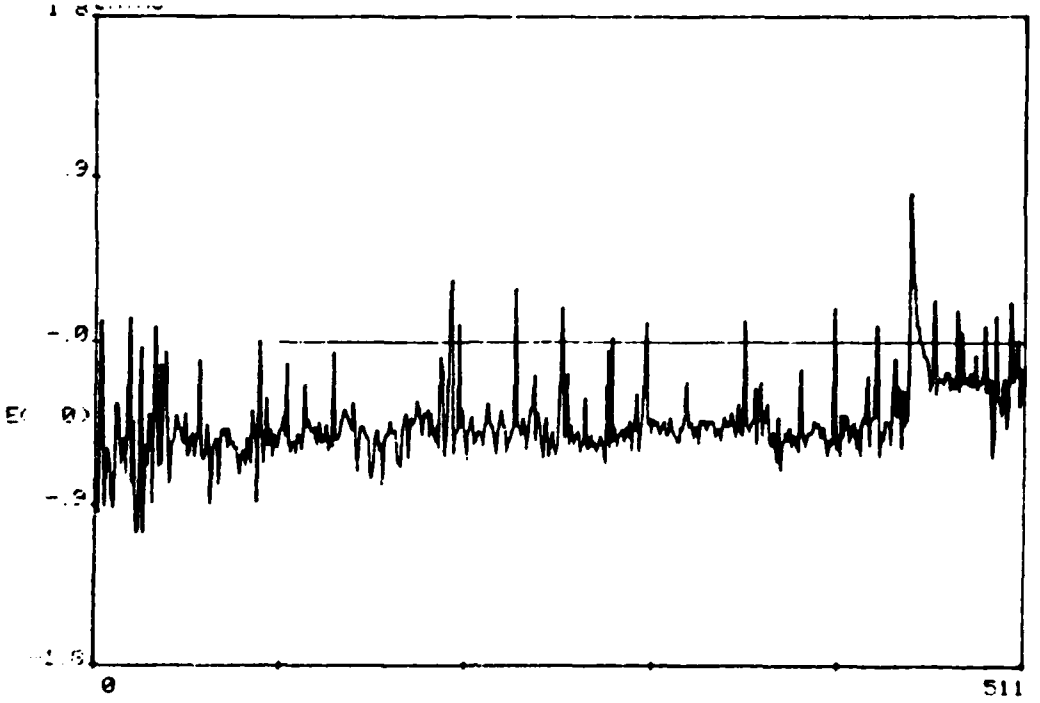


Figure G-4e: Columns 2 and 3; Row 4; Day 10; Blocks 21-24

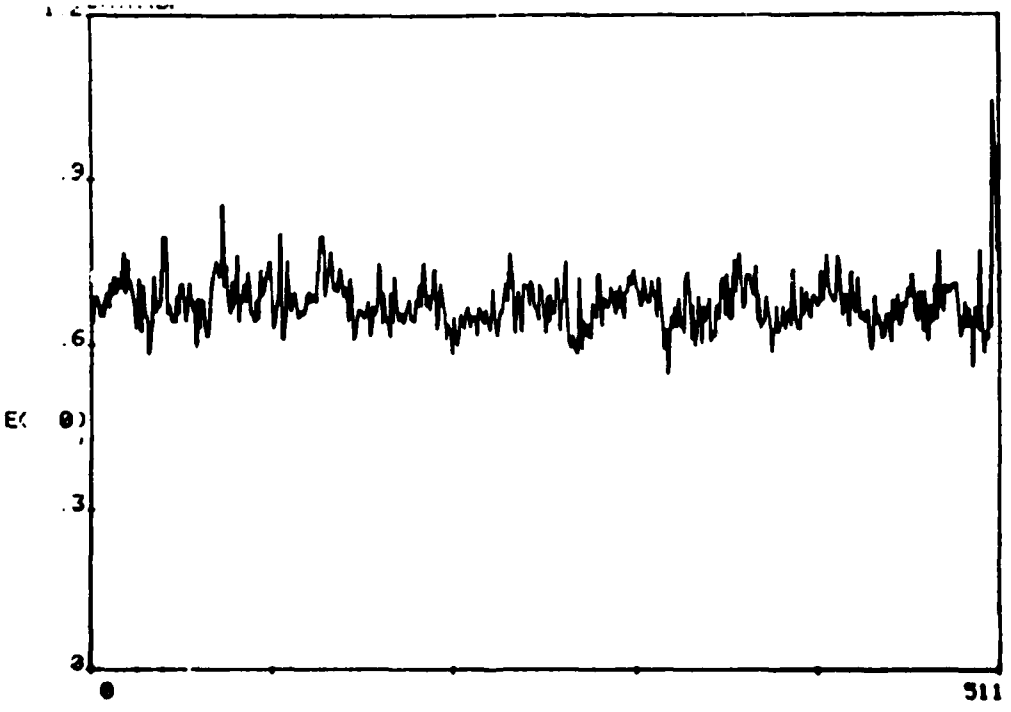


Figure G-5: Columns 2 and 3; Row 1; Day 6; Blocks 1-3

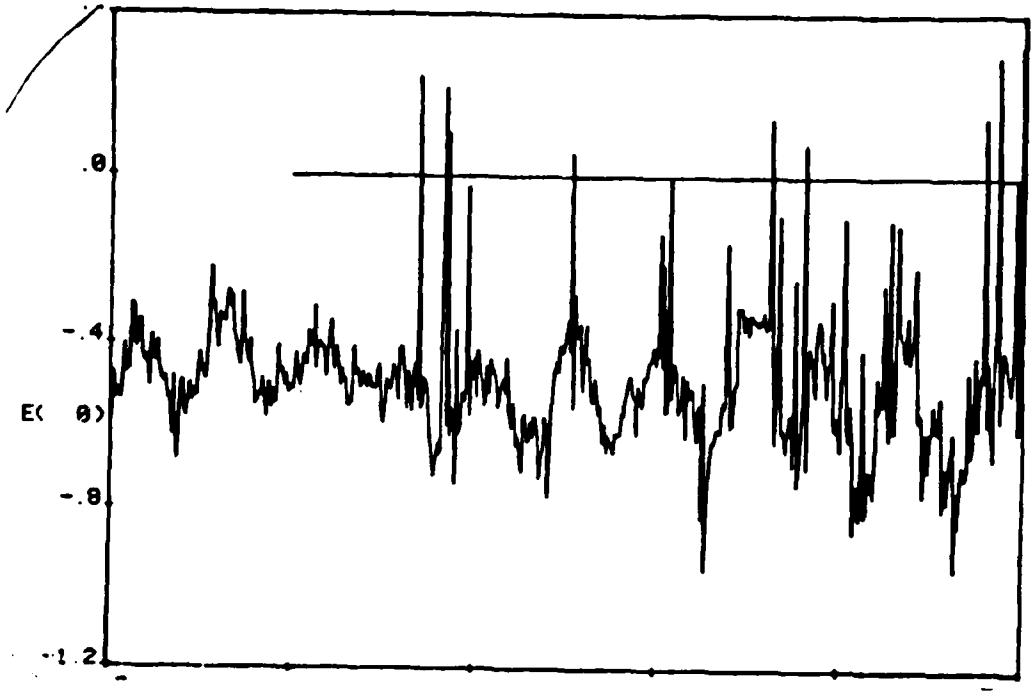


Figure G-6: Columns 2 and 3; Row 1; Day 3; Blocks 1-4

Figure G-7a: Columns 2 and 3; Row 1; Day 7; Blocks 5-8
(Plot Includes Strobe Signal)

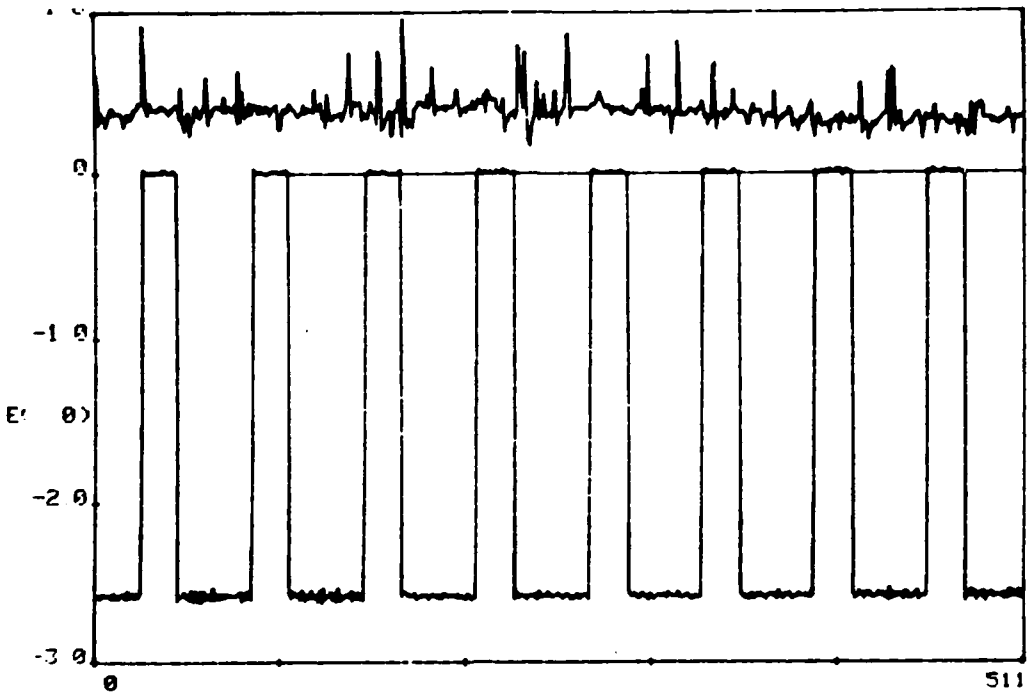


Figure G-7b: Columns 2 and 3; Row 1; Day 7; Blocks 9-12
(Plot Includes Strobe Signal)

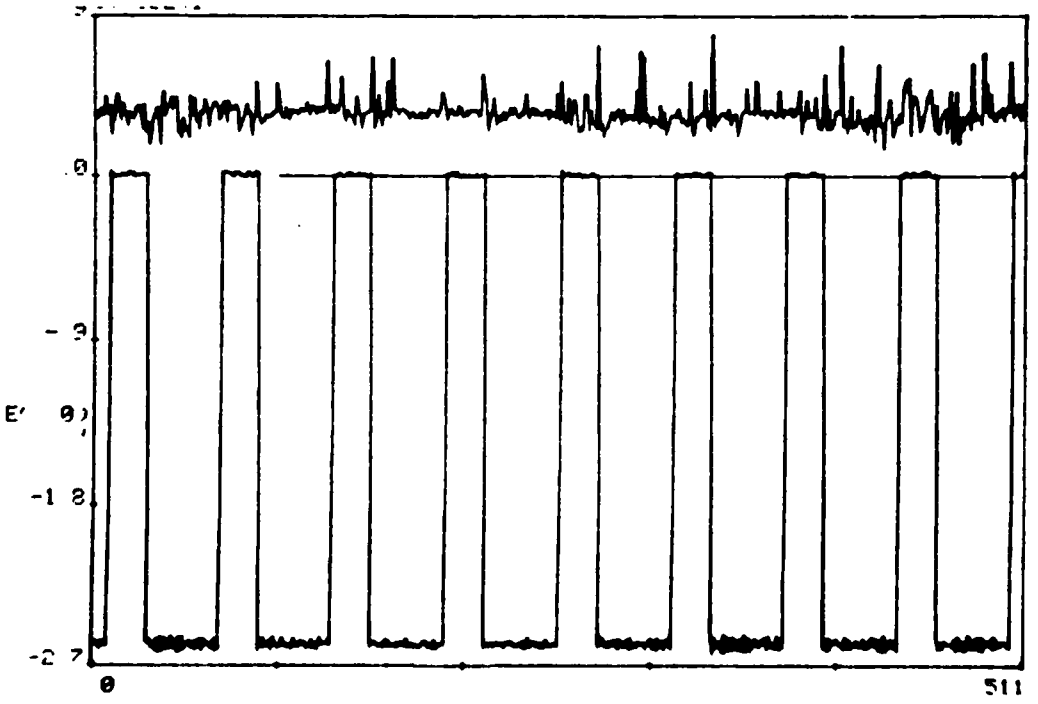


Figure G-7c: Columns 2 and 3; Row 1; Day 7; Blocks 13-16
(Plot Includes Strobe Signal)

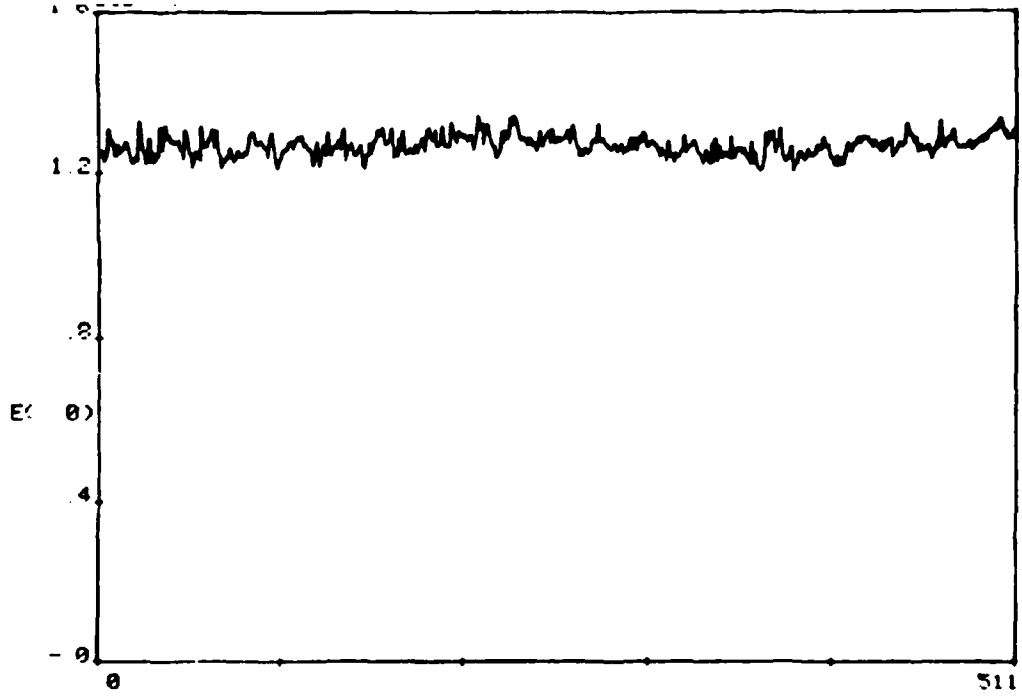


Figure G-8a: Columns 2 and 3; Row 2; Day 9; Blocks 7-10

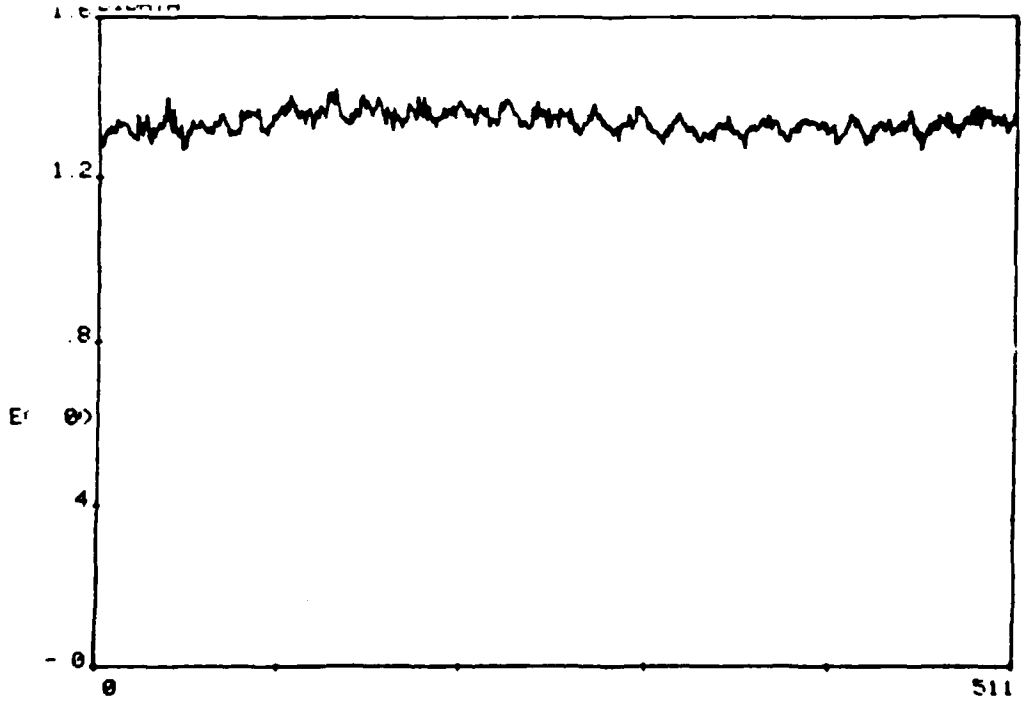


Figure G-8b: Columns 2 and 3; Row 2; Day 9; Blocks 11-14

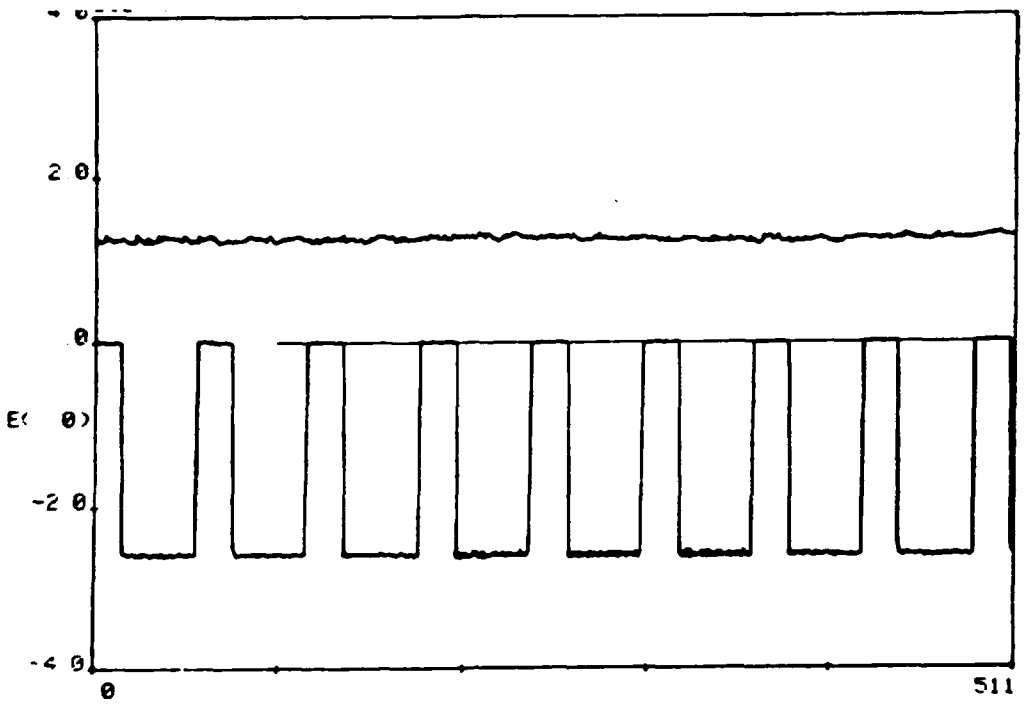


Figure G-8c: Columns 2 and 3; Row 2; Day 9; Blocks 7-10
(Plot includes Strobe Signal)

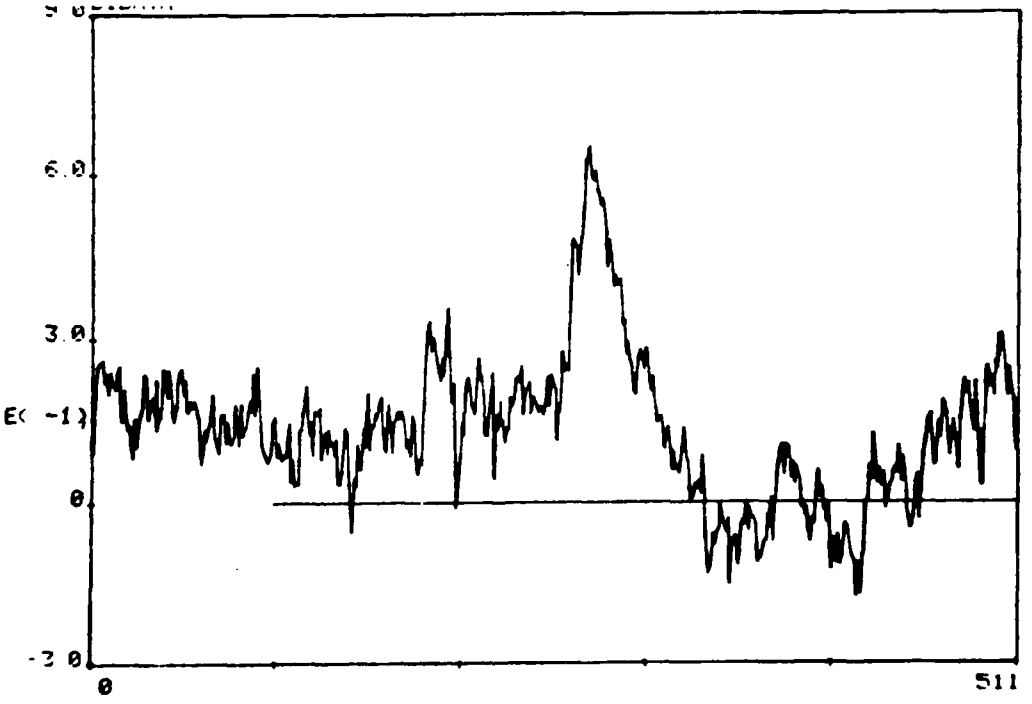


Figure G-9: Columns 2 and 3; Row 2; Day 13; Blocks 2-5

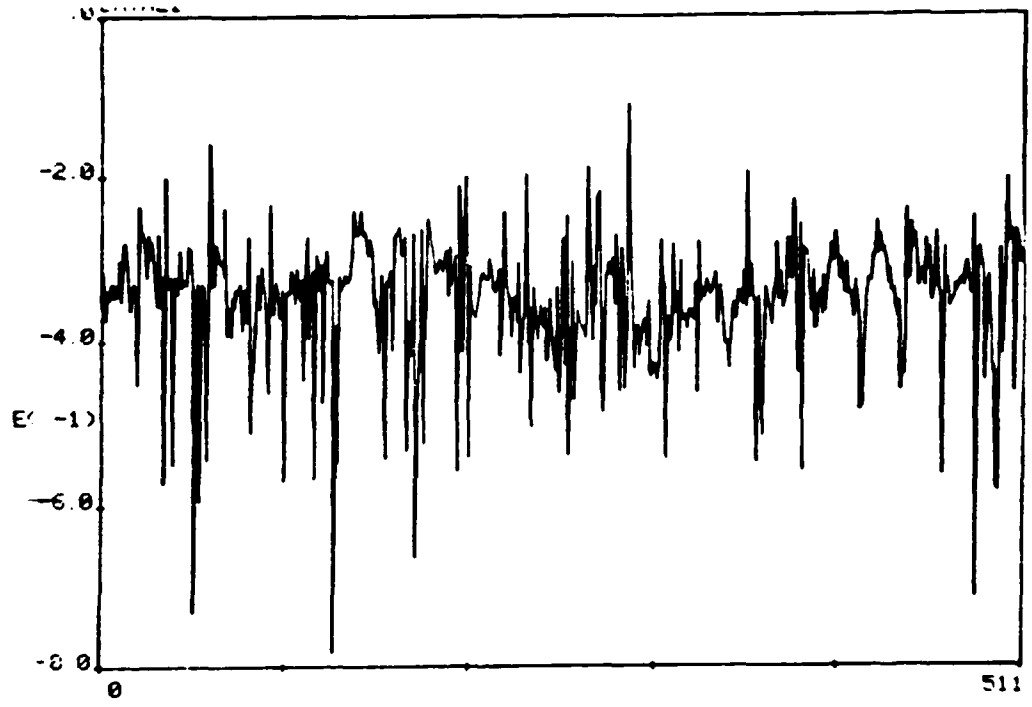


Figure G-10a: Columns 2 (absolute); Row 1; Day 12; Blocks 7-10

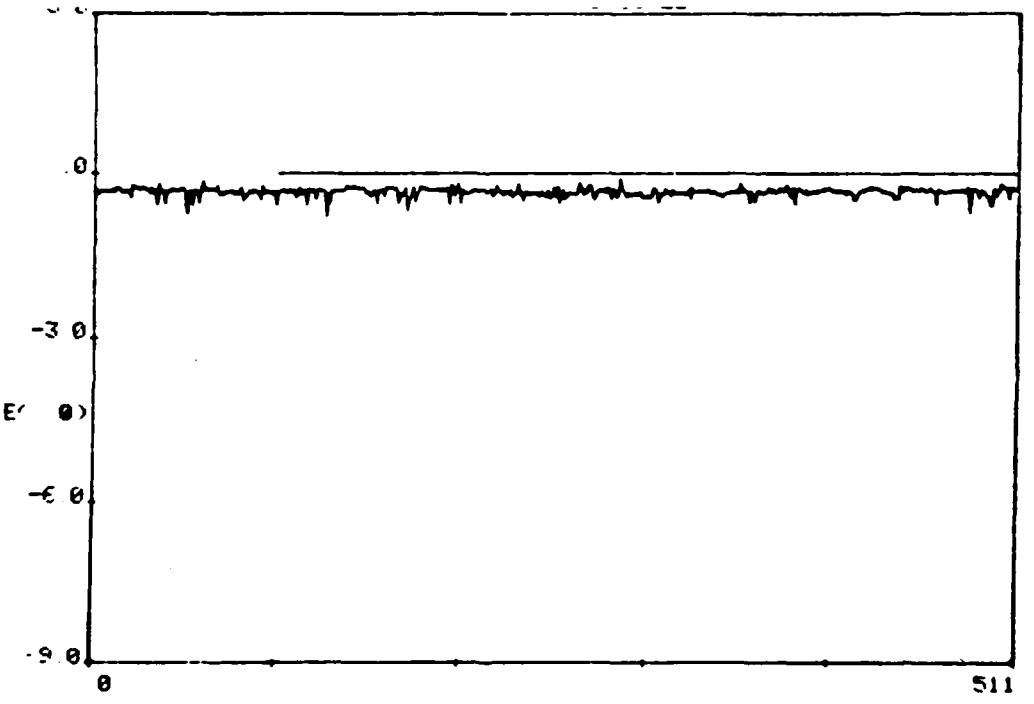


Figure G-10b: Columns 2 (absolute); Row 1; Day 12; Blocks 7-10
(Same as G-10a with scale reduction)

Figures G-11 through G-13 represent data which has been averaged using the program in Appendix G. In all cases the plot is 127 points or one block of data. This corresponds to one second. Figures G-11 and G-12 are plots of data collected differentially between sensing pads then averaged. Figure G-13 is a plot of data collected from an ear probe referenced to the L-shaped electrode on the AFIT array.

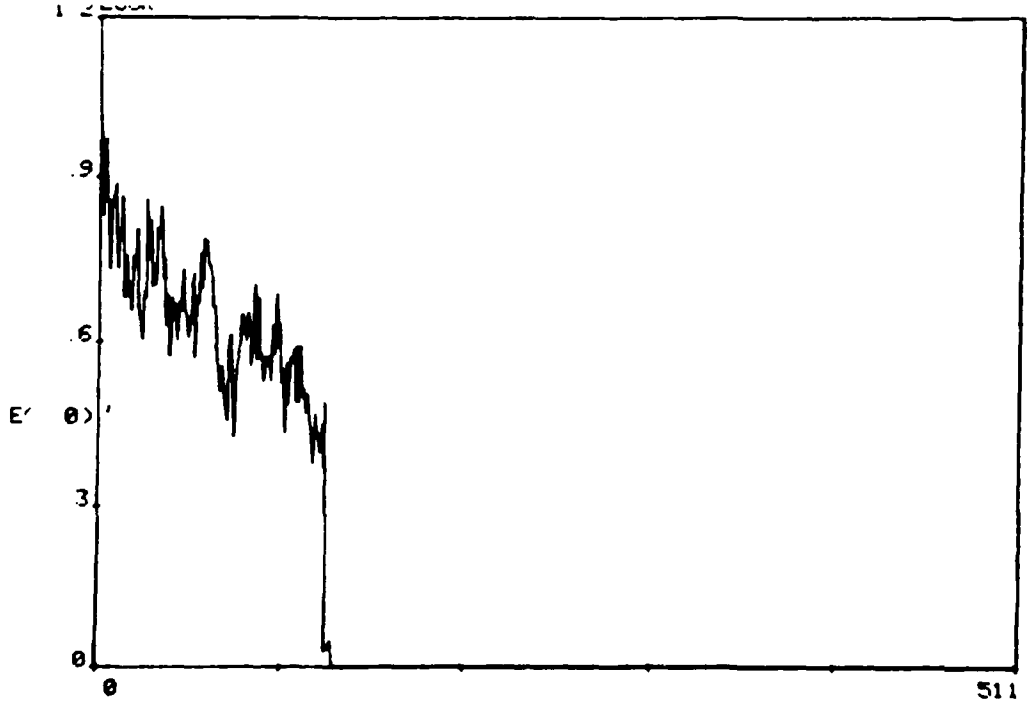


Figure G-11

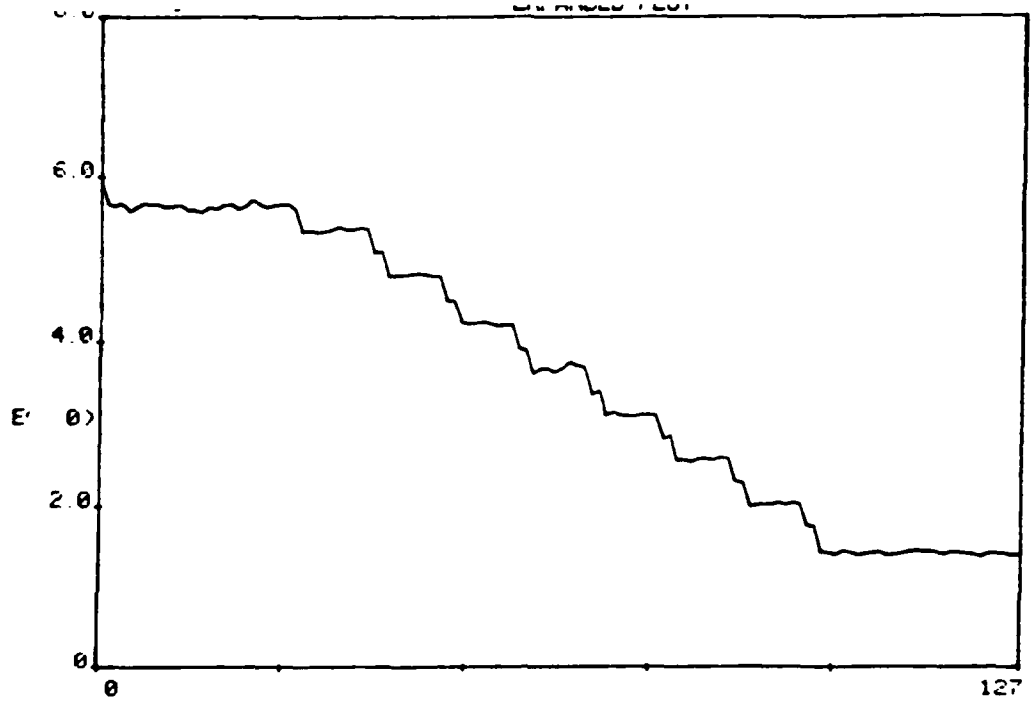


Figure G-12

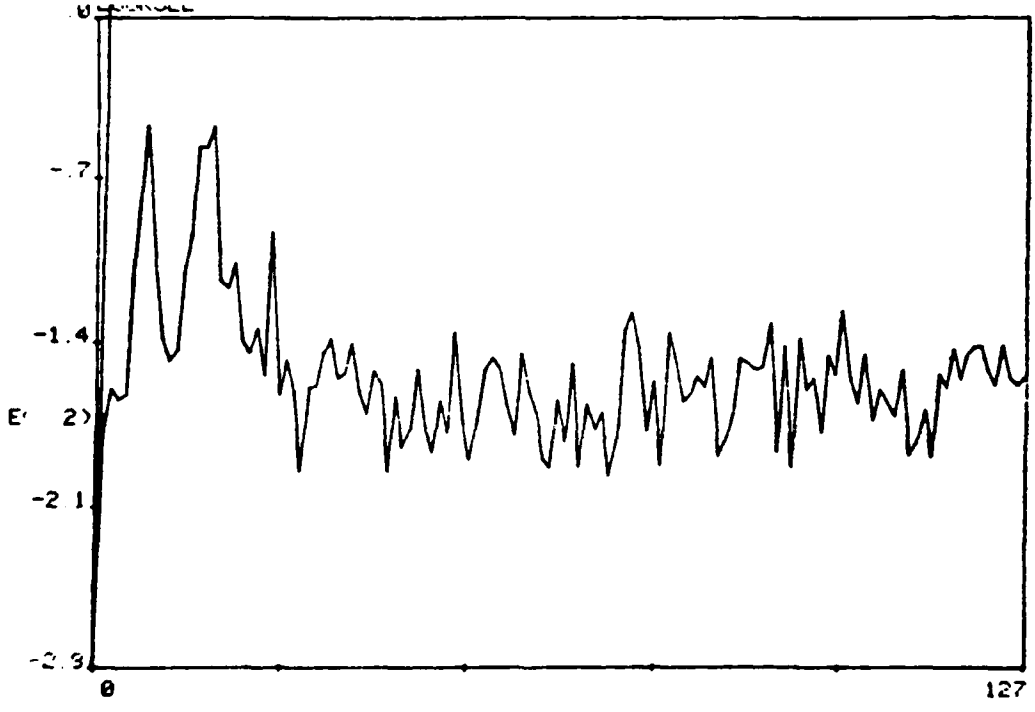


Figure G-13

APPENDIX B

INTRODUCTION

This appendix is included simply to identify two devices. It is not intended to imply that these schedules are absolutes but rather guidelines in some laboratories. Close comparison with appendix C will reveal many similarities. The reason being, both of these were used in developing the encapsulation process schedule.

STANDARD CLEAN

1.	Blow clean	Dry, pressurized nitrogen (N_2)
2.	Place wafer in solution--H_2SO_4/H_2O_2 3:2, let stand for ten minutes.	Clean Organic material
3.	Remove from solution, rinse in DI water to 10 megohms resistance.	Remove residual solution
4.	Place in solution-- DI water/HF, 10:1. Let stand for fifteen seconds then remove.	Inorganic clean.
5.	Remove from HF solution, rinse in DI water to 10 megohm resistance.	Removes residual HF solution.
6.	Dry two to three minutes.	

PHOTOLITHOGRAPHY PROCESS

1. Pre-dry wafers:	Insure proper adhesion of resist. (1 hour, 220 deg. C., N_2)
2. Spin on Photoresist:	Waycoat 28 cps (negative photo resist) 5000 rpm, 15 sec.
3. Pre-bake resist:	Prevents sticking to mask during alignment and exposure. (20 minutes, 70 deg. C.)
4. Mask alignment and exposure:	Resist is exposed to the pattern of the mask. Three to five sec., Ultra-violet.
5. Develop and rinse:	PR spin-spray developer. (propelant, N_2) 1- N_2, 30 sec. 2- Xylene, 30 sec. 3- Butyl acetate, 30 sec. 4- Dry N_2, 40 sec.
6. Inspection:	Check for proper development and alignment. Excess resist/small geometries not open--repeat step 5.
7. Coat back side:	Apply PR to back side of wafer.
8. Post-bake:	This step completes polymerization of the resist -insures proper adhesion between resist and oxide. (30 minutes, 150 deg. C.)
9. Inspection:	Examine to determine quality of resist, pinhole density, line width, and pattern definition. If too many large faults, resist must be removed and wafer reworked.

10.	Etch:	Pattern is etched into SiO_2 using a buffered HF solution at room temperature (4:1 NH_4F to HF).
11.	Inspection:	Determine if oxide has been completely removed and whether the etch has undercut the resist (windows pale white). Repeat etch step if necessary.
12.	Resist strip:	Plasma asher(O_2) 15 min.
13.	Final inspection:	Examine wafer with microscope to determine if PR has been totally removed.

NOTES:

--Etch one wafer at a time.

--Use care inserting wafer into etch so as not to cause air bubbles.

--Dry wafer thoroughly after etch rate inspection (step 11) then repeat only if necessary.

--Mix fresh etchant; let stand for one hour to chemically stabalize.

--If delay during etching, bake out for fifteen minutes at 150 degrees C. before continuing etch.

APPENDIX C

AFIT ARRAY ENCAPSULATION PROCESS

1.	Blow clean, N_2	Remove surface contaminants, dry.
2.	Spin on Polyimide (PI-2555/T-9035, 5:1)	3000 rpm, 15 seconds
3.	Initial cure	80° C., 30 minutes
4.	Spin on Photoresist	Negative PR (Waycoat 28 cps) 5000 rpm, 15 seconds
5.	Pre-bake resist	Prevents sticking to mask during alignment and exposure. 70 deg. C., 20 minutes.
6.	Mask alignment and exposure.	Resist is exposed to circuit pattern of the mask. 4.5 seconds exposure, Ultra Violet.
7.	Develop and rinse	PR spin-spray developer. 1 - N_2, 30 seconds. 2 - Xylene, 20 seconds 3 - Butyl acetate 35 seconds. 4 - Dry N_2, 40 seconds.
8.	Inspection	Check for proper development and alignment. Excess resist - small geometries - repeat step 7.
9.	Polyimide etch (positive photoresist developer; DI water/ AZ351, 1:5)	This step opens the contact windows and bonding pads. Puddle etchant on wafer wait five seconds, spin 60 seconds at 2000 rpm.Rinse with gentle DI water spray during spin.
10.	Dry	N_2 blow-off while spinning at 2000 rpm, 20 seconds.
11.	Inspection	Check for pattern definition, undercutting, excess polyimide repeat steps 9 and 10.

12. Post-bake	This step continues polymerization of the resist and continues PI cure.120deg. C. 20 minutes.
13. Return to step 2	Repeat procedure 3 to 5 times depending of film thickness desired.
14. Final cure	Completes PI cure 120 deg. C., 2 hours
15. Inspection	Check for defects and/or pattern integrity.
16. Wire bonding	Position wire, attach to bonding pad with silver contact paint.
17. Wire encapsulation (Dab PI over and around wires.)	Insure wires are secure and that there are no shorts between bonding pads. Repeat step 16 if necessary.
18. Initial cure	Cure 30 minutes at 80 deg. C. Repeat step 17 and 18 once.
19. Final cure	Complete PI polymerization 180 deg. C., 2 hours.
20. Inspection	Insure all contact points are well encapsulated.
21. Final prepartion	Bundle wire at point of back on wafer. Cover PI layer of step 17, chip edges and back plane with thin coat of epoxy glue for strength.
22. Final inspection	Insure only reference plane and 16 electrodes are exposed.

NOTES:

--Process one wafer at a time.

--Dry thoroughly after etch (step 9) before continuing etch.

--If electrodes show signs of residue of etchant place wafer in plasma asher for 3 minutes; repeat if necessary.

--Negative Photoresist stripper attacks PI, therefore, PR layer is left between PI layers.

--Insure wires are marked before bundling.

--Long cure times at reduced temperature may improve PI encapsulation.

APPENDIX D

INTEGRATED CIRCUIT DATA SHEETS

In the near future, technical data for the two integrated circuits used in this project may not be available. Therefore, complete specifications for both the MC14538B, Dual Prescision Retriggerable/Resettable Monostable Multivibrator, and the MC14022B, Octal Counter/Driver are provided here.

MOTOROLA
Semiconductors

MC14538B

McMOS MSI

(LOW POWER COMPLEMENTARY MOS)

DUAL PRECISION
RETRIGGERABLE/RESETTABLE
MONOSTABLE MULTIVIBRATOR

DUAL PRECISION RETRIGGERABLE/RESETTABLE MONOSTABLE MULTIVIBRATOR

The MC14538B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse and will produce an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X. Linear CMOS techniques allow more precise control of output pulse width.

- ±1.0% Typical Pulsewidth Variation from Part to Part
- ±0.5% Typical Pulsewidth Variation over Temperature Range
- New Formula: T = RC (T in seconds, R in ohms, C in farads)
- Pulse Width Range = 10 μs to ∞
- Symmetrical Output Sink and Source Capability
- Latched Trigger Inputs
- Separate Latched Reset Inputs
- Quiescent Current (Standby) = 5.0 nA/package typical @ 5 Vdc
- 3.0 Vdc to 18 Vdc Operational Limits
- Triggerable from Positive or Negative Going Edge
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-pin Compatible with MC14528B and CD4528 (CD4098)

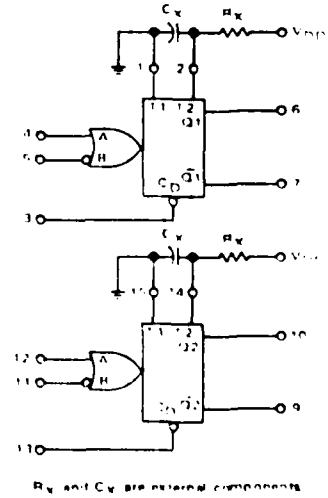
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix: Denotes
- L = Ceramic Package
- P = Plastic Package
- A = Extended Operating Temperature Range
- C = Limited Operating Temperature Range

BLOCK DIAGRAM



R_X and C_X are external components.

V_{DD} = Pin 16
V_{SS} = Pin 8

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	V
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	V
DC Current Drain per Pin	I	10	mA
Operating Temperature Range — AL, AP Device CL, CP Device	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage — 0 Level	V_{OL}	5.0		0.05	-	0	0.05		0.05	Vdc
V_{in} = V_{DD} or 0		10		0.05		0	0.05		0.05	
		15		0.05		0	0.05		0.05	
1 Level	V_{OH}	5.0	4.95		4.95	5.0		4.95		Vdc
V_{in} = 0 or V_{DD}		10	9.95		9.95	10		9.95	-	
		15	14.95		14.95	15		14.95	-	
Input Voltage# — 0 Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0		1.5		2.25	1.5		1.5	
(V_O = 9.0 or 1.0 Vdc)		10		3.0		4.50	3.0		3.0	
(V_O = 13.5 or 1.5 Vdc)		15		4.0		6.75	4.0		4.0	
1 Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5		3.5	2.75		3.5	-	
(V_O = 1.0 or 9.0 Vdc)		10	7.0		7.0	5.50		7.0	-	
(V_O = 1.5 or 13.5 Vdc)		15	11.0		11.0	8.25		11.0	-	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0		-2.4	-4.2		-1.7	-	
(V_{OH} = 4.6 Vdc)		5.0	-0.64		-0.51	-0.88		-0.36	-	
(V_{OH} = 9.5 Vdc)		10	-1.6		-1.3	-2.25		-0.9	-	
(V_{OH} = 13.5 Vdc)		15	-4.2		-3.4	-8.8		-2.4	-	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64		0.51	0.88		0.36	-	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6		1.3	2.25		0.9	-	
(V_{OL} = 1.5 Vdc)		15	4.2		3.4	8.8		2.4	-	
Output Drive Current (CL, CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5		-2.1	-4.2		-1.7	-	
(V_{OH} = 4.6 Vdc)		5.0	-0.52		-0.44	-0.88		-0.36	-	
(V_{OH} = 9.5 Vdc)		10	-1.3		-1.1	-2.25		-0.9	-	
(V_{OH} = 13.5 Vdc)		15	-3.6		-3.0	-8.8		-2.4	-	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52		0.44	0.88		0.36	-	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3		1.1	2.25		0.9	-	
(V_{OL} = 1.5 Vdc)		15	3.6		3.0	8.8		2.4	-	
Input Current, Pin 2 or 14	I_{in}	15		±0.02		±0.00001	±0.05		±0.5	µAdc
Input Current, Other Inputs, AL Device	I_{in}	15		±0.1		±0.00001	±0.1		±1.0	µAdc
Input Current, Other Inputs, CL, CP Device	I_{in}	15		±0.3		±0.00001	±0.3		±1.0	µAdc
Input Capacitance, Pin 2 or 14	C_{in}					25				pF
Input Capacitance, Other Inputs (V_{in} = 0)	C_{in}					5.0	7.5			pF
Quiescent Current (AL Device)	I_{DD}	5.0		5.0		0.005	5.0		150	µAdc
(Per Package)		10		10		0.010	10		300	
		15		20		0.015	20		600	
Quiescent Current (CL, CP Device)	I_{DD}	5.0		20		0.005	20		150	µAdc
(Per Package)		10		40		0.010	40		300	
		15		80		0.015	80		600	
Quiescent Current, Active State	I_{DD}	5.0				15				µAdc
(Q1 = Logic 1)		10				80			-	
(Q2 = Logic 0)		15				125				
**Total Supply Current at an external load capacitance (C_L) and an external timing network (R_x, C_x)	I_T	5.0	$I_T = (2.5 \times 10^{-2}) R_x C_x f + 40 C_x f + 1 \times 10^{-5} C_L f$							
		10.0	$I_T = 5 \times 10^{-2} R_x C_x f + 80 C_x f + 2 \times 10^{-5} C_L f$							
		15.0	$I_T = 7.25 \times 10^{-2} R_x C_x f + 120 C_x f + 3 \times 10^{-5} C_L f$							
			where: I_T = A (minimum total supply current), C_x = µF, C_L = pF, R_x = k ohms, and f = the input frequency.							

*T_{low} = -55°C for AL Device, -40°C for CL, CP Device
T_{high} = +125°C for AL Device, +85°C for CL, CP Device
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 V min @ V_{DD} = 5.0 V
2.0 V min @ V_{DD} = 10 V
2.5 V min @ V_{DD} = 15 Vdc
**The formulas given are for the typical characteristics only at 25°C

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ	Max	
Output Rise Time	t_r					ns
t_r = (1.35 ns/pF) C_L + 33 ns		5.0		100	200	
t_r = (0.60 ns/pF) C_L + 20 ns		10		50	100	
t_r = (0.40 ns/pF) C_L + 20 ns		15		40	80	
Output Fall Time	t_f					ns
t_f = (1.35 ns/pF) C_L + 33 ns		5.0		100	200	
t_f = (0.60 ns/pF) C_L + 20 ns		10		50	100	
t_f = (0.40 ns/pF) C_L + 20 ns		15		40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
A or B to Q or $\overline{Q}$						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 255 ns		5.0		300	600	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 132 ns		10		150	300	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 97 ns		15		100	220	
C_D to Q or $\overline{Q}$						ns
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 205 ns		5.0		250	500	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 107 ns		10		125	250	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 82 ns		15		95	190	
Minimum Input Pulse Width	PW_{in}	5.0		15	70	ns
A, B or C_D		10		30	60	
		15		25	50	
Minimum Retrigger Time	t_{rr}	5.0	0			ns
		10	0			
		15	0			
Output Pulse Width, Q or $\overline{Q}$	T					μs
Refer to Figure 8 for other values of R_x and C_x						
C_x = 0.002 μF, R_x = 100 kΩ		5.0	217	222	234	
		10	217	224	236	
		15	224	226	238	
C_x = 0.1 μF, R_x = 100 Ω		5.0	9.5	9.86	10.4	ms
		10	9.6	10	10.5	
		15	9.6	10.14	10.7	
C_x = 10 μF, R_x = 100 kΩ		5.0	0.915	0.965	1.15	s
		10	0.93	0.98	1.01	
		15	0.94	0.99	1.04	
Pulse Width Match between circuits in the same package $\frac{T_2 - T_1}{T_1}$ C_x = 0.1 μF, R_x = 100 kΩ		5.0		±1		%
		10		±1		
		15		±1		

OPERATING CONDITIONS

External Timing Resistance	R_x		5.0		*	kΩ
External Timing Capacitance	C_x		No limit		No limit	μF

*The maximum usable resistance R_x is a function of the leakage of the capacitor C_x, leakage of the MC14538B, and leakage due to board layout and surface resistance.

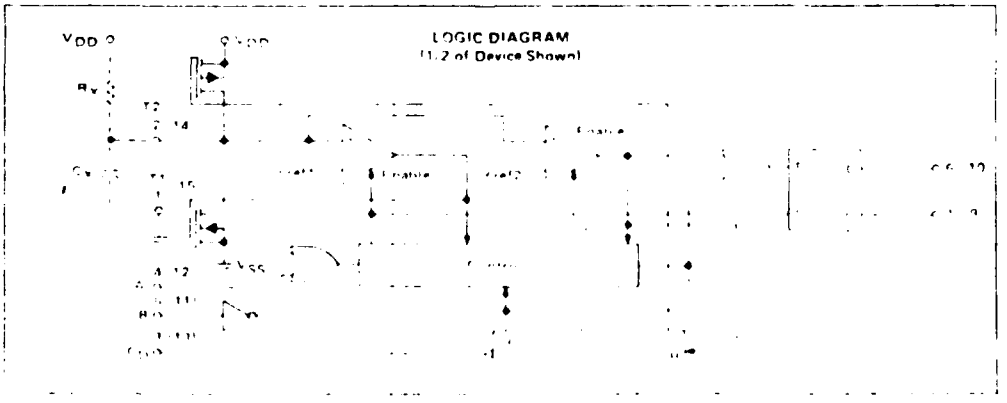


FIGURE 1 POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

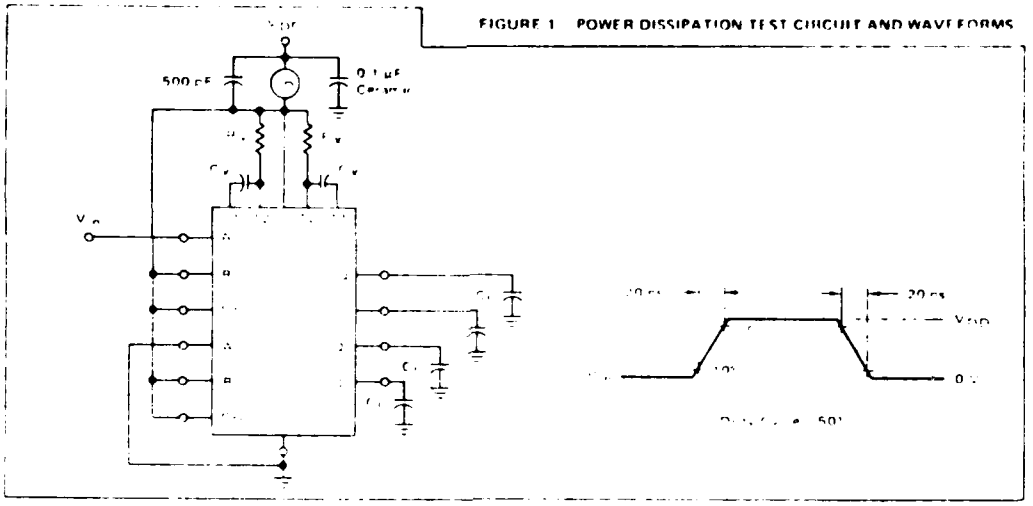
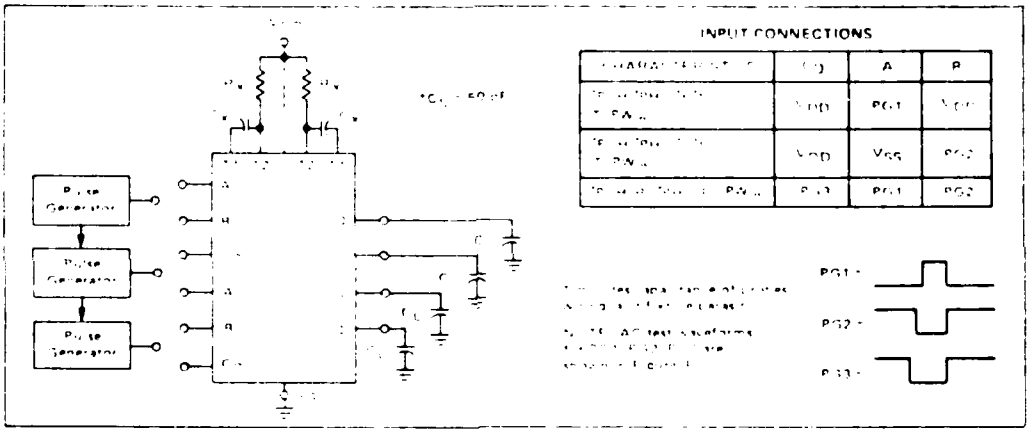


FIGURE 2 - AC TEST CIRCUIT



INPUT CONNECTIONS

		A	B
	V_{DD}	PG1	
	V_{DD}	V_{SS}	PG2
		PG1	PG2

FIGURE 3 - AC TEST WAVEFORMS

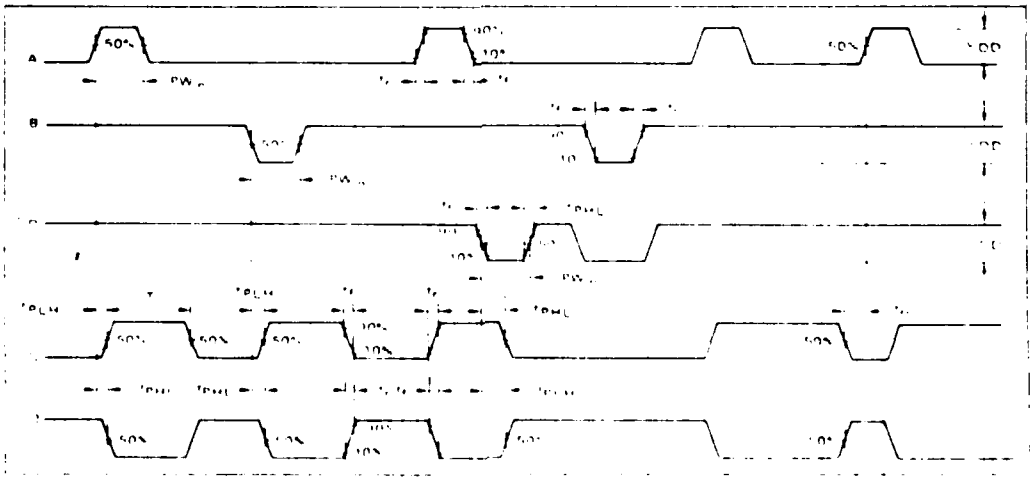


FIGURE 4 – TYPICAL NORMALIZED DISTRIBUTION OF UNITS FOR OUTPUT PULSE WIDTH

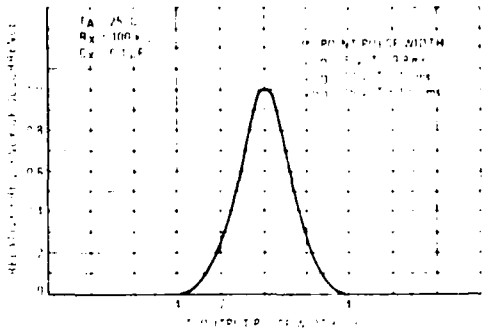


FIGURE 5 – TYPICAL PULSE WIDTH VARIATION AS A FUNCTION OF SUPPLY VOLTAGE V_{DD}

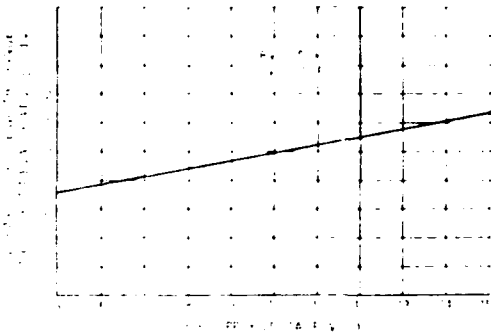


FIGURE 6 – TYPICAL TOTAL SUPPLY CURRENT versus OUTPUT DUTY CYCLE

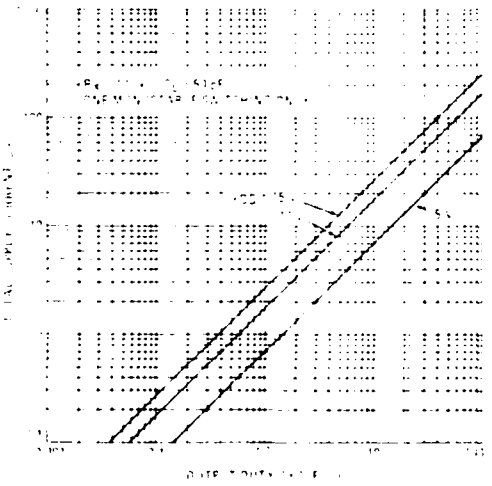


FIGURE 7 – TYPICAL PULSE WIDTH ERROR versus TEMPERATURE

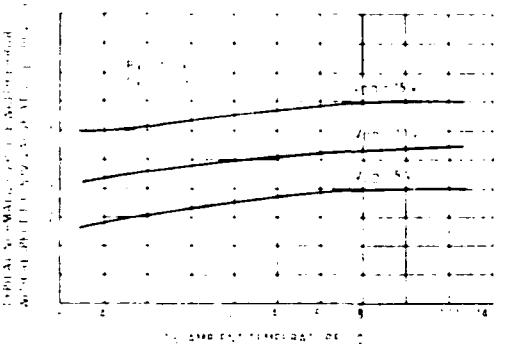


FIGURE 8 – TYPICAL PULSE WIDTH ERROR versus TEMPERATURE

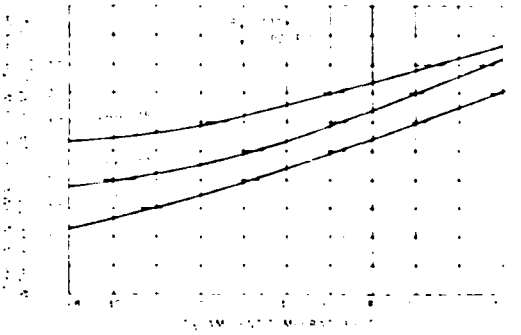
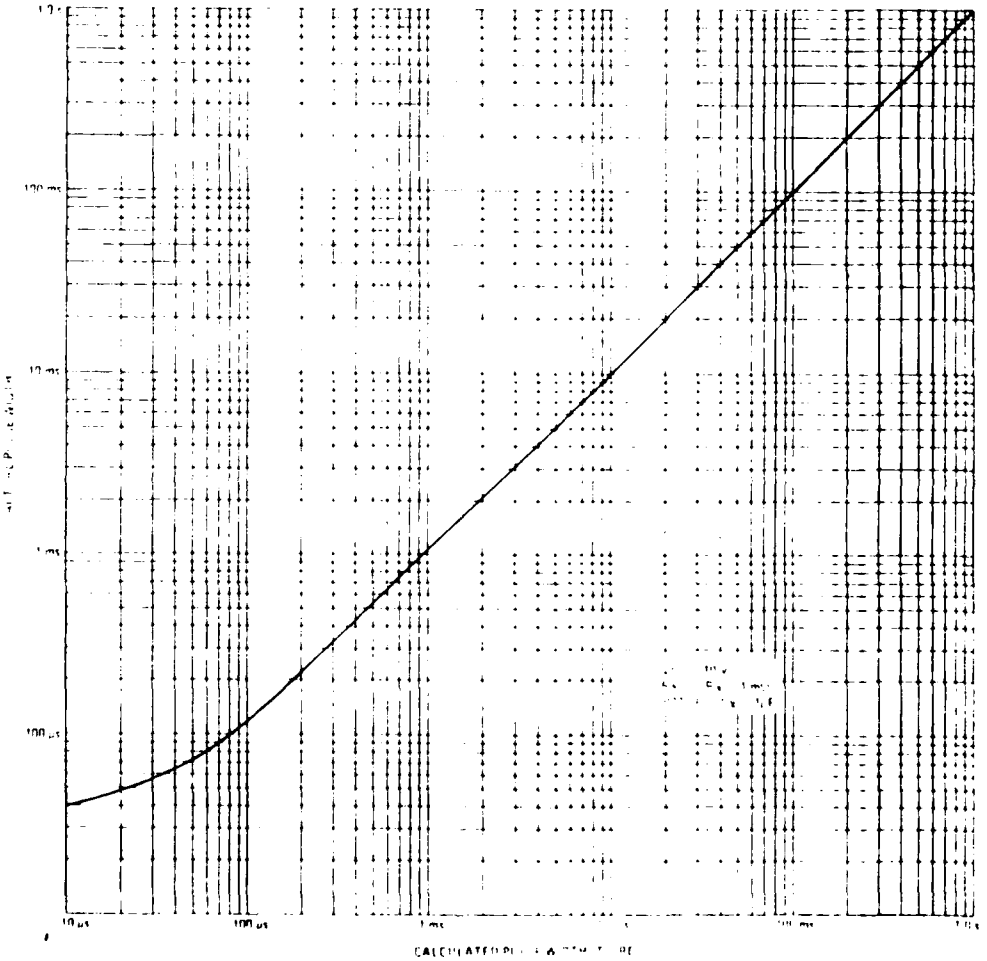


FIGURE 9 - TYPICAL PULSE WIDTH versus T = RC



MOTOROLA
semiconductor

MC14022AL
MC14022CL
MC14022CP

McMOS

LOW POWER COMPLEMENTARY MOS

OCTAL COUNTER/DIVIDER

L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

OCTAL COUNTER/DRIVER

The MC14022 is a [illegible] stage Johnson octal counter with built-in code converter. High speed operation and spike-free output decoding are achieved by use of a Johnson octal counter design. The eight decoded outputs are normally low and go high only at their appropriate octal time period. The output changes occur on the positive going edge of the clock pulse. This part can be used in frequency division applications as well as octal counter and octal decode display applications. Additional characteristics are [illegible] in the Family Data Sheet.

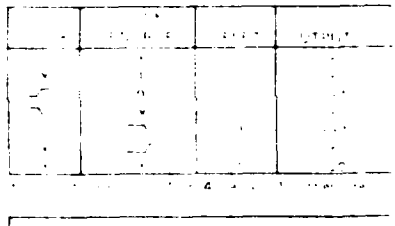
- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- 12 MHz (typical) Operation — V_{DD} = 10 Vdc
- Divide-by-N Counting Achieved with MC14001 NOR Gate
- Pin for Pin Replacement for CD4022A

MAXIMUM RATINGS [illegible]

Rating	Symbol	Value	Unit
[illegible] MC14022AL MC14022CL, CP	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]
[illegible] P MC14022AL MC14022CL, CP	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]

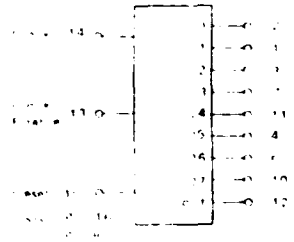
FUNCTIONAL TRUTH TABLE

[illegible]



LOGIC DIAGRAM

BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq$ [illegible] $\leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

[illegible]

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage 0 Level	V_{out}	5.0		0.01		0	0.01	-	0.05	Vdc
		10		0.01		0	0.01	-	0.05	
		15		0.05		0	0.05	-	0.25	
1 Level		5.0	4.99		4.99	5.0		4.95		Vdc
		10	9.99		9.99	10		9.95		
		15	14.95		14.95	15		14.75	-	
Noise Immunity#	V_{NL}									Vdc
($V_{out} \leq 0.8$ Vdc)		5.0	1.5		1.5	2.25		1.4	-	
($V_{out} \leq 1.0$ Vdc)		10	3.0		3.0	4.50		2.9	-	
($V_{out} \leq 1.5$ Vdc)		15	4.5		4.5	6.75		4.4	-	
($V_{out} \leq 0.8$ Vdc)	V_{NH}	5.0	1.4		1.5	2.25		1.5	-	Vdc
($V_{out} \leq 1.0$ Vdc)		10	2.9		3.0	4.50		3.0	-	
($V_{out} \leq 1.5$ Vdc)		15	4.4		4.5	6.75		4.5	-	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62		-0.50	-1.1		-0.35	-	
(V_{OH} = 9.5 Vdc)		10	-0.62		-0.50	-1.1		-0.35	-	
(V_{OH} = 13.5 Vdc)		15	-1.8		-1.5	-3.5		-1.1	-	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.50		0.40	0.88		0.28		mAdc
(V_{OL} = 0.5 Vdc)		10	1.1		0.90	2.0		0.65		
(V_{OL} = 1.5 Vdc)		15	4.2		3.4	8.0		2.4		
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.23		-0.20	-0.41		-0.16		
(V_{OH} = 9.5 Vdc)		10	-0.23		-0.20	-0.41		-0.16		
(V_{OH} = 13.5 Vdc)		15	-0.69		-0.60	-1.35		-0.48		
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23		0.20	0.41		0.16		mAdc
(V_{OL} = 0.5 Vdc)		10	0.60		0.50	1.0		0.40		
(V_{OL} = 1.5 Vdc)		15	1.8		1.5	3.5		1.2		
Input Current	I_{in}	-				-				μAdc
Input Capacitance (V_{in} = 0)	C_{in}	-				5.0				pF
Quiescent Dissipation (AL Device)	P_D	5.0		0.025		0.0015	0.025		1.5	mW
		10		0.10		0.006	0.10		6.0	
		15		0.30		0.015	0.30		18	
Quiescent Dissipation (CL/CP Device)	P_D	5.0		0.25		0.0015	0.25		1.5	mW
		10		1.0		0.006	1.0		14	
		15		3.0		0.015	3.0		42	
Power Dissipation**	P_D	5.0	$P_D = (0.64 \times 10^{-3} f + 0.5 \times 10^{-6} f) V_{DD}^2$							mW
Dynamic plus Quiescent		10	$P_D = (1.2 \times 10^{-3} f + 2.0 \times 10^{-6} f) V_{DD}^2$							
(C_L = 15 pF)		15	$P_D = (3.1 \times 10^{-3} f + 5.0 \times 10^{-6} f) V_{DD}^2$							

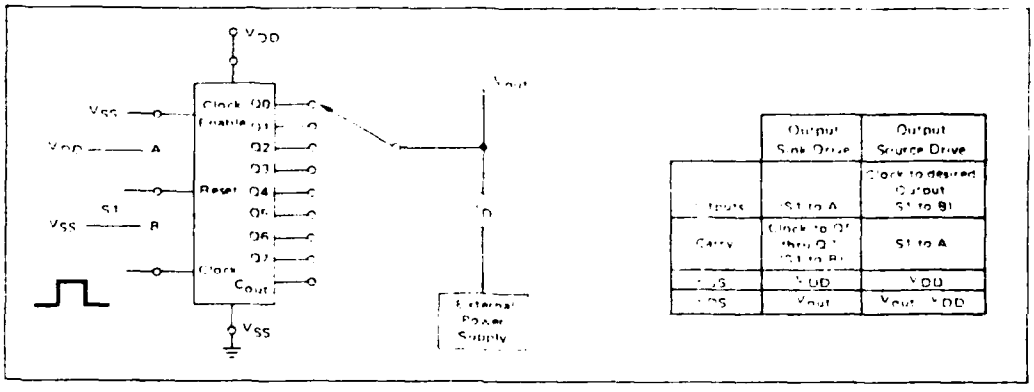
*T_{low} = -55°C for AL Device, -40°C for CL/CP Device
T_{high} = +125°C for AL Device, +85°C for CL/CP Device
#Noise immunity specified for worst-case input combination.
*For dissipation at different frequency, output loading or supply voltage, C_L use the formula
$P_T (C_L) = P_D + 1.25 \times 10^{-3} f (C_L - 15\text{pF}) V_{DD}^2$
where P_T, P_D in mW (per package), C_L = [illegible], V_{DD} = [illegible], f = [illegible] frequency.
**The formula given is for the typical characteristic only.

SWITCHING CHARACTERISTICS* (T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min AL Device	Min CL/CP Device	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Output Rise Time (C_L = 15 pF)	t_r							ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0			70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10			35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15			25	55	80	
Output Fall Time (C_L = 15 pF)	t_f							ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0			70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10			35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15			25	55	80	
Propagation Delay Time (C_L = 15 pF)	t_{PLH}							ns
Reset to Decode Output*	t_{PHL}							
t_{PLH}, t_{PHL} = (2.0 ns/pF) C_L + 420 ns		5.0			450	800	1200	
t_{PLH}, t_{PHL} = (0.9 ns/pF) C_L + 186.5 ns		10			200	400	500	
t_{PLH}, t_{PHL} = (0.7 ns/pF) C_L + 109.5 ns		15			120	300	375	
Propagation Delay Time (C_L = 15 pF)	t_{PLH}							ns
Clock to C_{out}	t_{PHL}							
t_{PLH}, t_{PHL} = (2.0 ns/pF) C_L + 320 ns		5.0			350	550	700	
t_{PLH}, t_{PHL} = (0.9 ns/pF) C_L + 111.5 ns		10			125	250	300	
t_{PLH}, t_{PHL} = (0.7 ns/pF) C_L + 74.5 ns		15			85	190	225	
Propagation Delay Time (C_L = 15 pF)	t_{PLH}							ns
Clock to Decode Output	t_{PHL}							
t_{PLH}, t_{PHL} = (2.0 ns/pF) C_L + 455 ns		5.0			485	720	940	
t_{PLH}, t_{PHL} = (0.9 ns/pF) C_L + 166.5 ns		10			180	360	400	
t_{PLH}, t_{PHL} = (0.7 ns/pF) C_L + 114.4 ns		15			125	270	300	
Turn Off Delay Time (C_L = 15 pF)	t_{PLH}							ns
Reset to C_{out}								
t_{PLH} = (2.0 ns/pF) C_L + 320 ns		5.0			350	750	1000	
t_{PLH} = (0.9 ns/pF) C_L + 111.5 ns		10			125	250	300	
t_{PLH} = (0.7 ns/pF) C_L + 69.5 ns		15			80	190	225	
Minimum Clock Pulse Width	PW_C	5.0			100	200	250	ns
		10			42	70	100	
		15			30	55	75	
Maximum Clock Frequency	f_{RF}	5.0	2.5	2.0	5.0			MHz
		10	7.0	5.0	12			
		15	9.0	6.7	16			
Minimum Reset Pulse Width	PW_R	5.0			200	380	500	ns
		10			100	165	250	
		15			75	125	190	
Reset Removal Time	t_{rem}	5.0			300	500	750	ns
		10			100	200	275	
		15			80	150	210	
Maximum Clock Input Rise and Fall Time (C_L = 15 pF)	t_r, t_f	5.0	No Limit	No Limit		-	-	-
		10				-	-	
		15				-	-	
Clock Enable Setup Time (C_L = 15 pF)	t_{setup}	5.0			175	300	700	ns
		10			75	150	300	
		15			52	115	225	
Clock Enable Release Time (C_L = 15 pF)	t_{rel}	5.0			240	400	700	ns
		10			100	200	300	
		15			70	150	225	

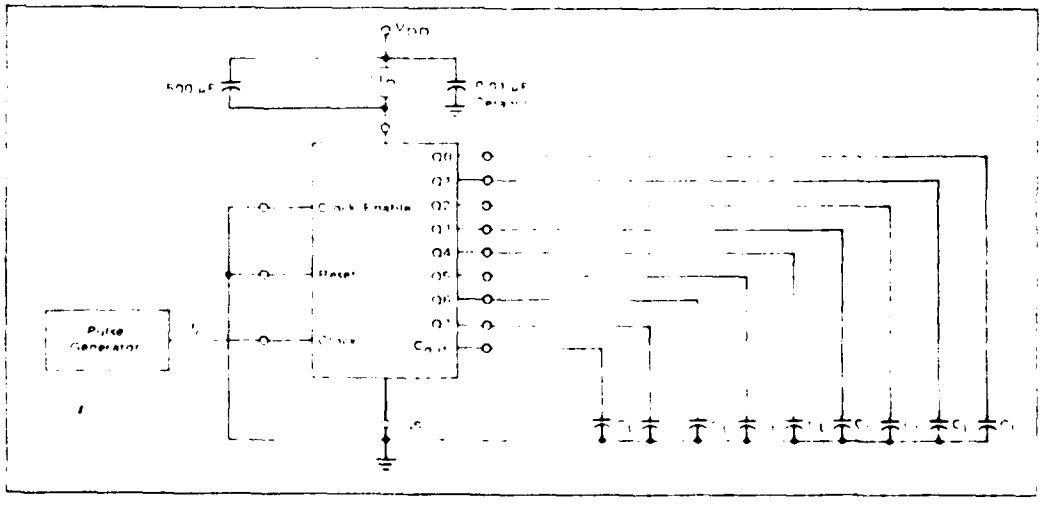
*The formula given is for the typical characteristics only.

FIGURE 1 – TYPICAL OUTPUT SOURCE AND OUTPUT SINK CHARACTERISTICS TEST CIRCUIT



	Output Sink Drive	Output Source Drive
Inputs	S1 to A	Clock to desired Q output S1 to B1
Carry	Clock to Q7 thru Q1 S1 to B1	S1 to A
VSS	VDD	VDD
VDS	Vout	Vout - VDD

FIGURE 2 – TYPICAL POWER DISSIPATION TEST CIRCUIT



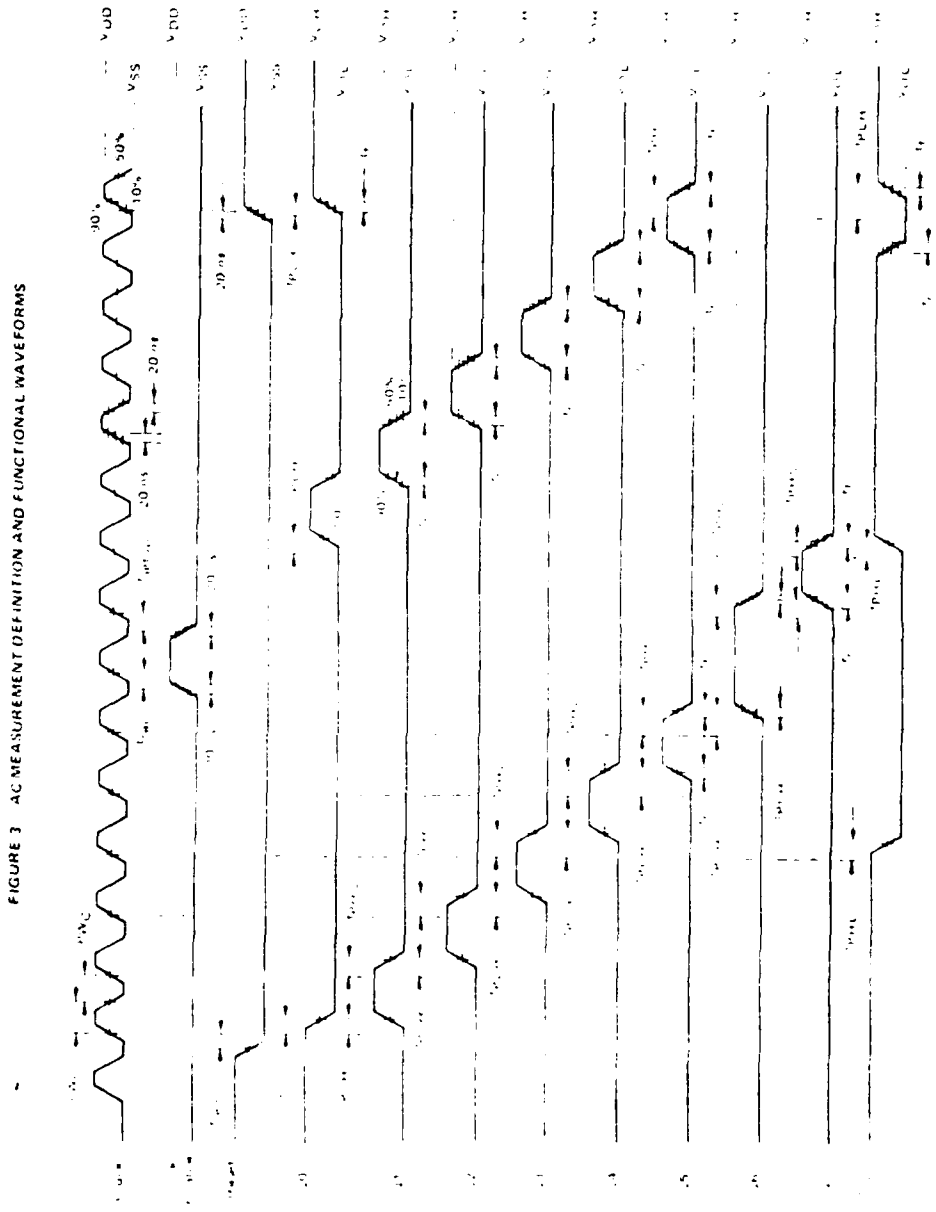
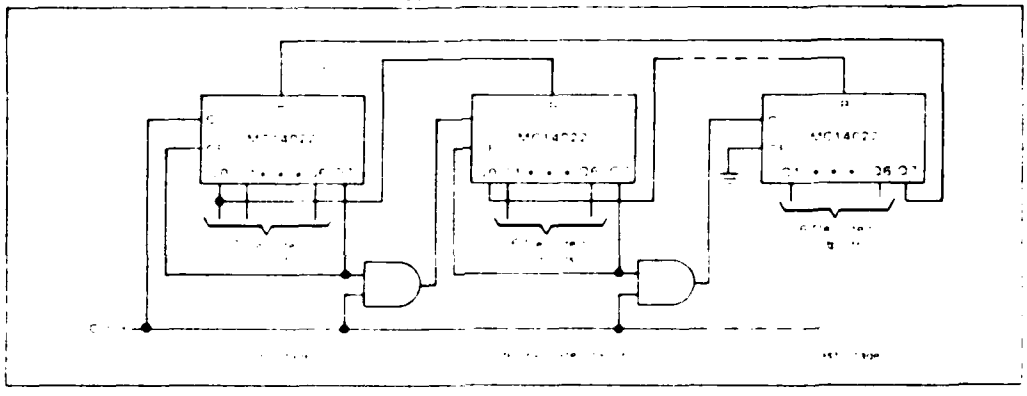


FIGURE 3 - AC MEASUREMENT DEFINITION AND FUNCTIONAL WAVEFORMS

APPLICATIONS INFORMATION

Figure 4 shows a technique for extending the number of decoded output states for the MC14022. Decoded outputs are sequentially true each stage and from stage to stage with no dead time (except propagation delay).

FIGURE 4 – COUNTER EXPANSION



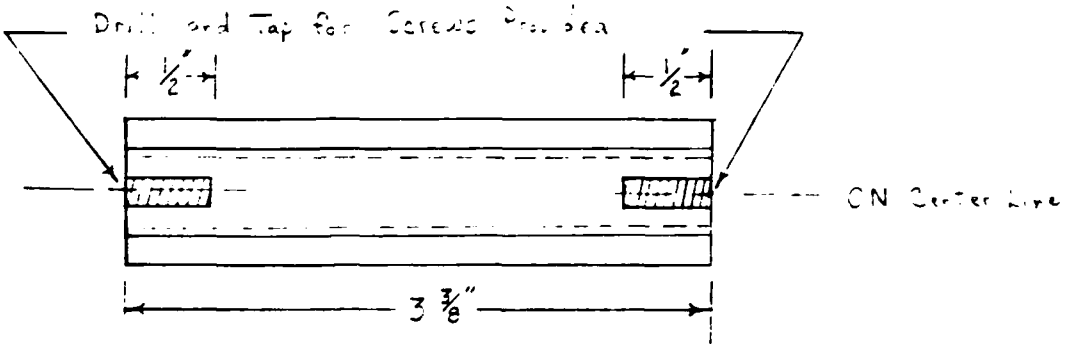
APPENDIX E

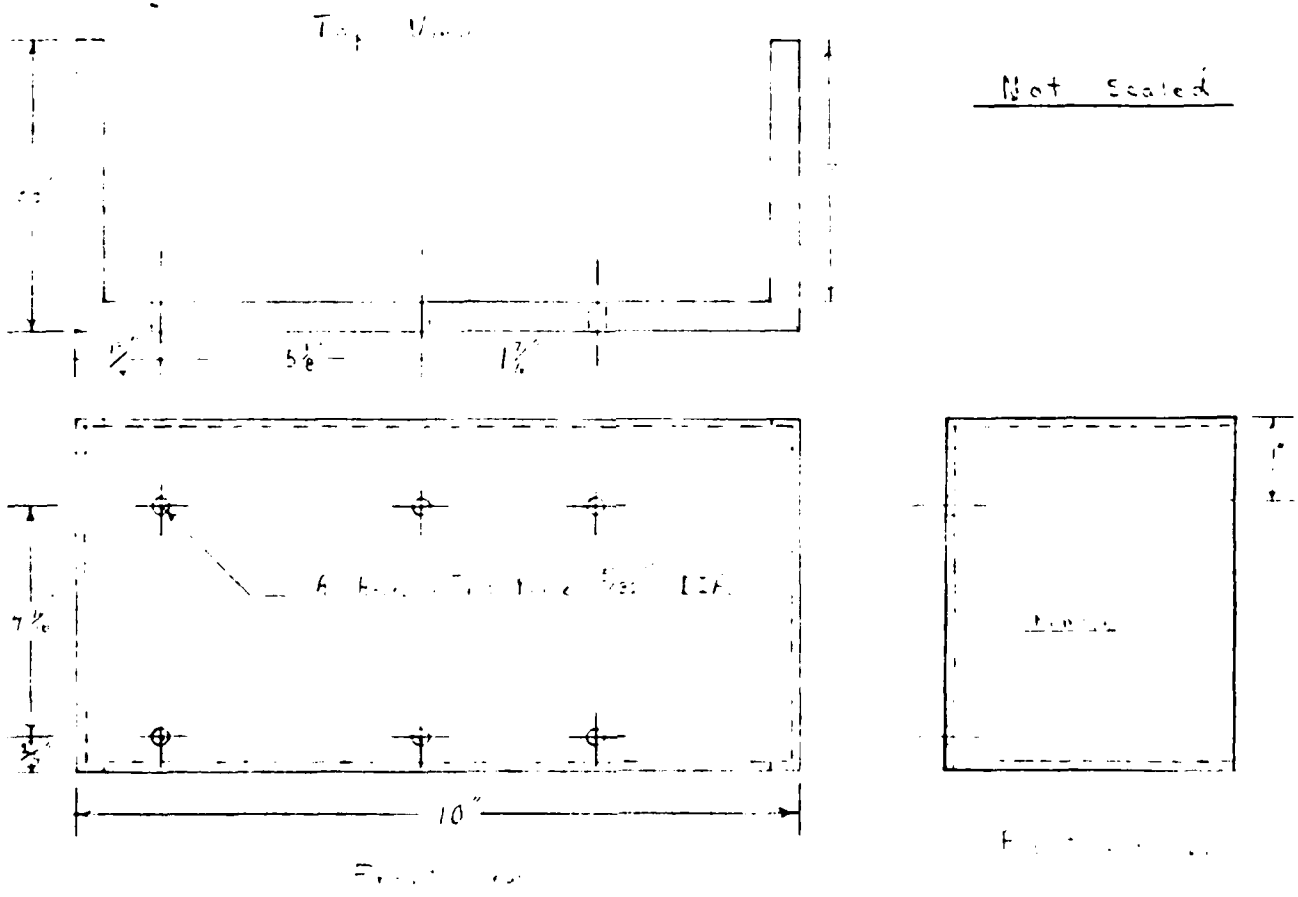
CHASSIS MECHANICAL DRAWINGS

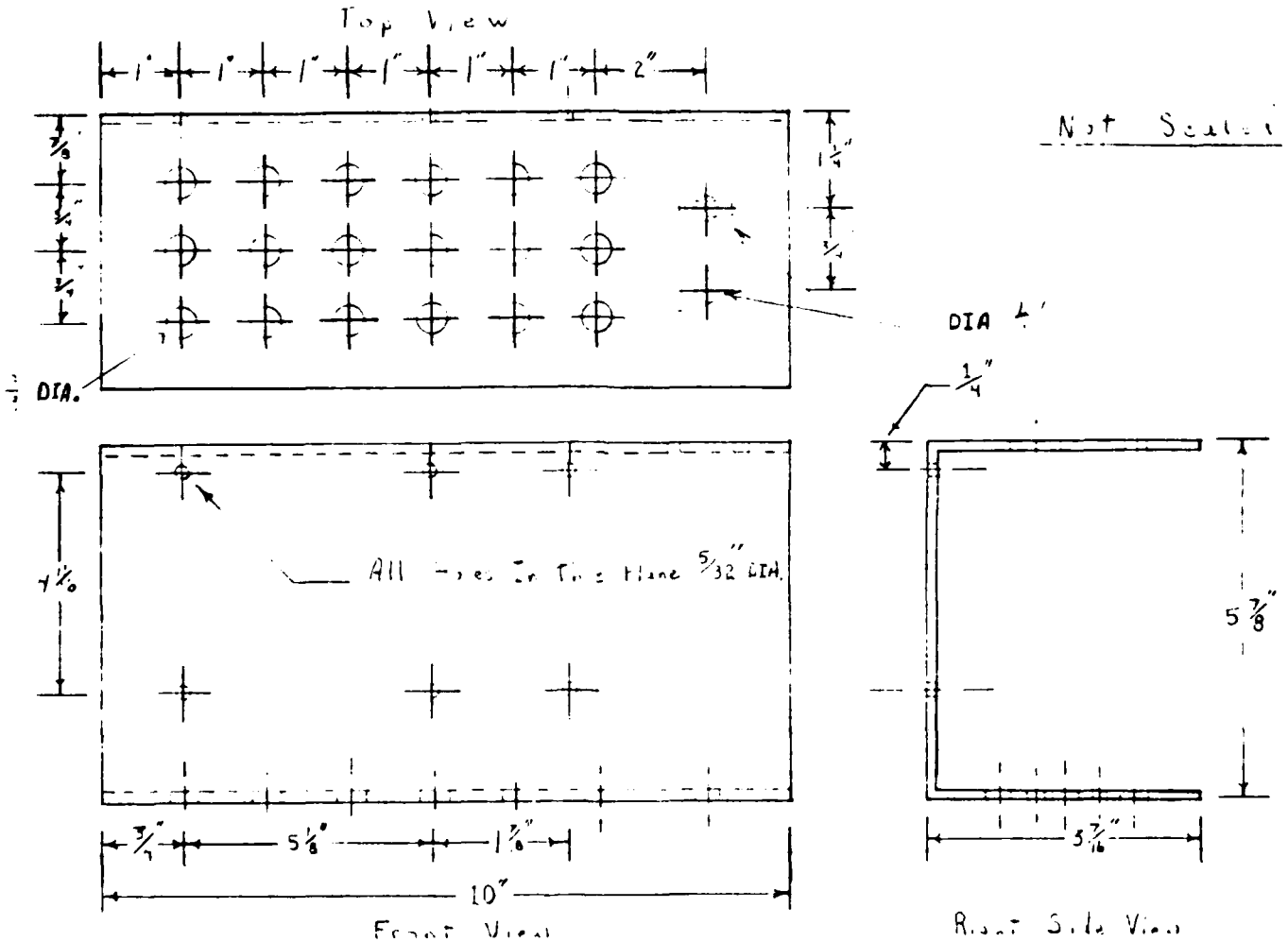
The External Drive Circuit Chassis was designed to be extremely compact. Card Cage and connector locations were selected to provide maintainability and electrical shielding.

Hole sizes and location will depend on the type and size of screws and card cage used. Holesize of a standard BNC connector is 3/8 inch.

Card Cage Supports




Not Scaled
10"


Top View
1" 1" 1" 1" 1" 1" 2"
Not Scale
DIA.
DIA
1/4"
All Holes In This Plane 5/32" DIA.
10"
Front View
Right Side View

APPENDIX F

COMMERCIALLY PRODUCED INTEGRATED CIRCUIT

The AFIT multielectrode array used for this research was made by AFIT students with the cooperation of the Air Force Avionics Laboratory. Their endeavor produced about ten wafers of nine arrays each. But not all of the chips were usable. Yet, the creation of the first functional chip was a major accomplishment for a totally "non-standard" process.

However, during his research German discovered a few minor problems (Ref. 7). First, the operating characteristics of each JFET were uniquely different. In some cases, differing by orders of magnitude. Of particular importance were the pinch-off voltage Vp, the leakage current at pinch-off, and the on-resistance. German surmized that the students making the chip were probably not experienced in the field of semiconductor techniques and equipment. An experienced technician is an essential part of making semiconductors by a "standard" process. Such experience is even more essential for creating an integrated circuit by "nonstandard" processes. Therefore, some of the problems found in the AFIT multielectrode array may have been induced by the student without his knowledge.

For example, the surface of some chips showed signs of contamination; probably caused by delays during the fabrication process. Primarily, because a student does not have the continuous time required to process a wafer to

completion. Whereas, a wafer under "standard" process is usually processed to completion without interruption or unnecessary delay.

Thus, German recommended that a commercial firm be engaged to process the wafers. The experience found in a commercial foundry should :

1) Standardize JFET Characterisics
2) Improve JFET Characteristics
3) Improve Chip Quality
4) Improve the "yield"
5) And Permit Modifications to the Chip.

After surveying foundries in the United States, talks were initiated with the Microelectronics Division of the National Cash Register Company of Dayton, Ohio. Representatives of the National Cash Register Company did considerable research into the AFIT process and development of the chips. It was their opinion that the overall quality of the chips could be improved while increasing the yield by a factor of twenty or more. This is possible because of the tremendous accuracy of their equipment and because they use four inch wafers. In addition, they were prepared to provide the engineering necessary to set the pinch-off voltage and insure standardized JFET characteristics.

National Cash register Company representatives also raised questions about AFIT array metalization. The AFIT

process uses a chrome-platinum-gold metalization layer. Since their standard process uses aluminum, they recommended using silver on aluminum as the total metalization layer. If this process could be realized, it would offer a significant advantage since silver-chloride has proved to be a very good conductor of cortical signals in other research.

Finally, these gentlemen were receptive to our suggested additions to the basic chip (i.e the addition of the multiplex drive circuitry). In the original AFIT array design, a large portion of the space available on the chip is unused. The addition of the multiplex circuitry to the chip would simplify operation of multiple chips and increase reliability.

Representatives of the National Cash Register Company (NCR) and the United States Air Force reached a tenative agreement to make a modified version of the AFIT multi-electrode array.

ON-CHIP MULTIPLEX CIRCUITRY

This thesis endeavor involved many parallel efforts. One effort conducted by three AFIT students under the direction of Captain Roger Colvin involved the design of a multiplex or counter circuit and its addition to the original AFIT multielectrode array. The counter must generate the four "row" signals based on an externally provided clock. It must also be capable of operating many AFIT multielectrode arrays in parallel. The multiplexing circuit requires a VDD of +6 volts DC and a VSS of -6 volts

volts and is used for reference. If necessary, this modified array can be driven by an external circuit. In such a case, the on chip multiplexer is disabled by connecting the +6 volts, -6 volts and neutral to -6volts.

Additional constraints are mentioned in the report of LT's Robert Bellacico, Jayme LaVoie and Wilfred Posten. The authors of this thesis are extremely grateful to these gentlemen. Further, their success has contributed greatly to the development of a modified AFIT Multielectrode Array. Their report follows.

EE 6.95 PROJECT

14 JUNE 1982

GROUP #1

2 LT. ROBERT BELLACICCO

2 LT. JAYME LaVOIE

2 LT. WILFRED POSTEN

TABLE OF CONTENTS

BACKGROUND

At the present time, very little is known about the interaction between the eyes and the brain of an animal. to determine how the brain interprets the data received from the eyes, scientists are pursuing several catagories of research. This report concerns the approach used in Dr. Kabrisky's research and that of several AFIT theses. This approach consists of providing an input to the eyes of an animal (by placing pictures in front of it) and then measuring its brain's electrical response (through an array of electrodes placed flat against an area of the cortex which is known to take part in the vision proces). Through analysis of this recorded data, scientists expect to gain insight into the actual signal processing aspect of vision. A future goal of this effort is an understanding of the vision process in humans.

As mentioned, electrical impulses from the brain will be sampled through the use of an array of electrodes. This array was designed by Lt. Tatman. And subsequently, modified and fabricated by Capt. Fitzgerald. The design consists of 16 electrodes arranged in a 4 X 4 array. Each electrode has an n-channel JFET located next to it which either passes the electrode voltage or blocks it. Each one of the 4 row inputs controls 4 of the 16 JFET's. When a row is turned on, an output signal is available at each of the column outputs. So, by sampling the column lines at 4 times the rate of the clocking circuit for row inputs, all 16 electrodes can be sequentially sampled. A version of this

array is shown in Figure 1.

PROBLEM STATEMENT

This project entails the addition of a counter circuit which will sequence through the 4 row inputs, turning one row on at a time. This counter will be constructed of N-channel JFET's on silicon, just as the electrode switches are, and will be integrated onto the same chip as the electrode array.

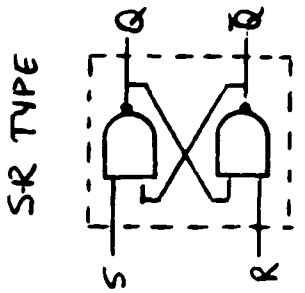
The circuit inputs will be +6 volts, -6 volts, a clock signal and a synchronization input. And the outputs will be the four data outputs, a ground reference, a substrate reference and a synchronization output.

Group #1 of the EE 6.95 class is providing the design for this counter circuit to National Cash Register (NCR) Company in Miamisburg who will provide AFIT with a copy of the circuit mask set. Then both NCR and Group #1 will fabricate copies of the circuit. AFIT's fabrication efforts will be conducted in building 125, the Processing Laboratory.

CRITERIA FOR THE DESIGN

The environment the circuit will operate in is highly saline, and sodium ions are very mobile. Due to these ions, a device which is resistant to impurities was needed. Thus Lt. Tatman chose JFET's as switches. Since the junction is located within the substrate, JFET's are more immune than other transistors.

INITIAL DESIGN
RING COUNTER



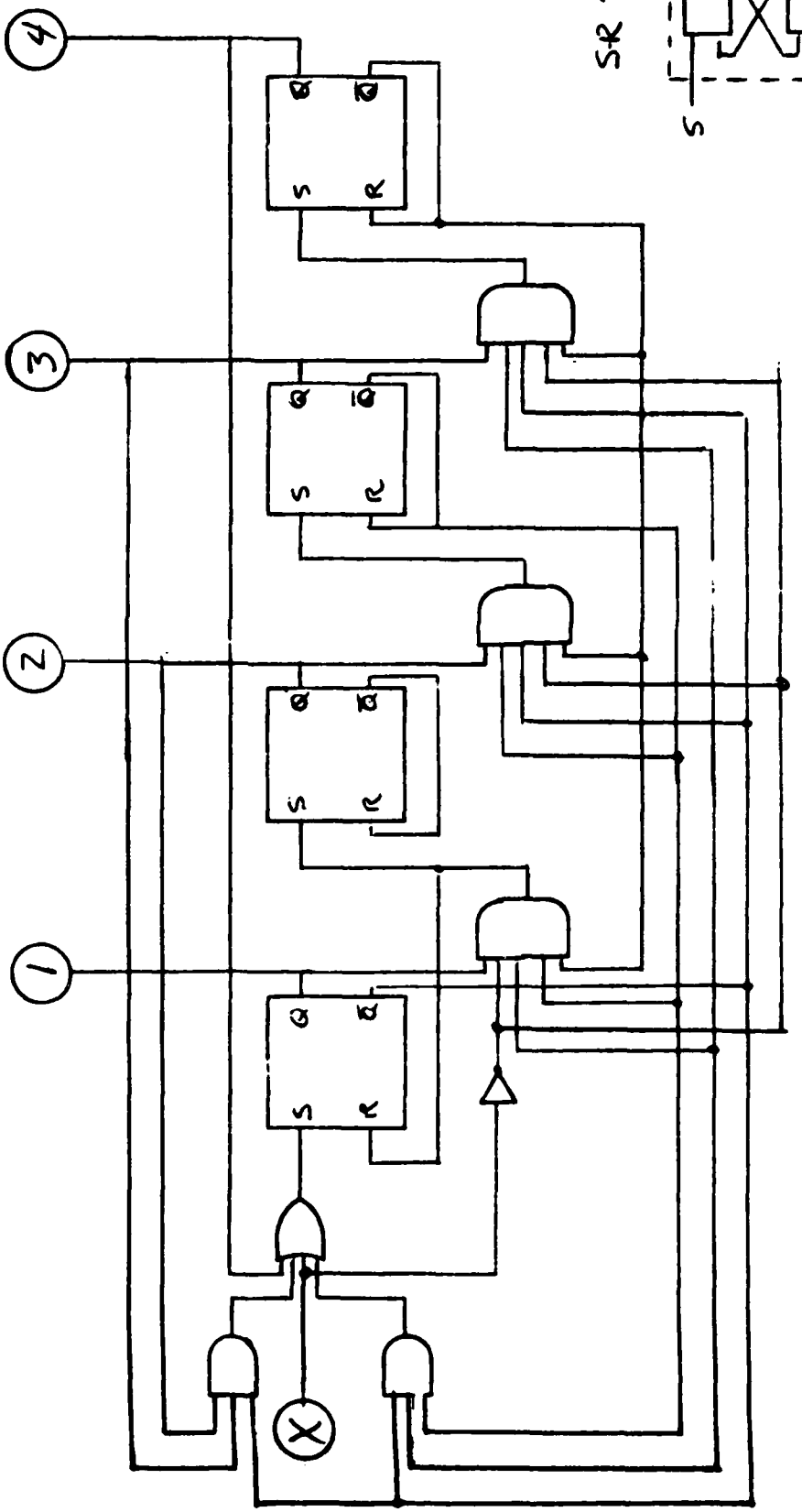


Figure 2

Also, the expected voltage level on the brain's surface is a few microvolts. So, Lt. Tatman had to use switches with very low noise characteristics; JFET's provide this. And finally, for clean switching, a high off impedance is needed. Once again, this characteristic is provided by JFET's.

DEVELOPMENT OF THE DESIGN

When we started this project it was suggested that we implement a Johnson (or Ring) Counter, restricting it to just the four states required to obtain the desired ripple output. Our design required 4 R-S flip-flops since four outputs were required. Also, a number of multiple input gates were required for the reset circuitry. Figure 2 shows the original design using the four R-S flip-flops.

This initial design was rejected for a number of reasons, even though it did work with Transistor-Transistor Logic (TTL). A primary objective was to minimize the number of JFET's required. With this circuit, and our basic JFET logic gates, it would require 90 transistors to implement it. That is, 90 transistors for nonedge-triggered flip-flops. This brings up another problem. We found the output to be dependent on the frequency and duty cycle of the input. This is intolerable in the operation of the circuit. To eliminate this dependency we dediced to go with edge triggered flip-flops.

To implement an edge triggered flip-flop, we used the standard NAND gate implementation, found in a TTL Databook,

for D-Type flip-flops. If we were to stay with the ring 2 counter using the edge triggered flip-flop, the number of JFET's required would have risen to well over 150. Such a large number of transistors seemed impractical.

It was decided that since an edge trigered flip-flop required so many transistors, the thing to do then would be to attempt to decrease the number of flip-flops. This was done by using two flip-flops and a decoder to obtain the four states. The final design contains only 86 transistors, is edge triggered and uses only two types of gates (19 NAND and 1 AND). Figure 3 shows this final design. Also, Figure 4 shows how the NAND and AND gates are implemented with JFET's. For completeness Figure 5 shows the NOR and OR gates. Figure 6 (foldout) is a circuit diagram of the circuit implemented. And finally, Figure 7 is a photograph of the output displayed on an oscilloscope.

JFET DESIGN

After working with the discrete N-channel JFET's in the construction of our bread-board circuit, we were able to predict the operation of a load pair in a logic gate. It was found that if the uper load's saturation current is about 10% greater than the lower load's, the gate would almost always work, provided the proper number of diodes were used and the switches were also working. With this knowledge, we went forward with our calculations of the required geometry for our circuit JFET's. We used the same geometery for the upper loads and switches that were used

for the switches in the array. And to obtain the smaller saturation current for the lower load we used a shorter gate width. All this is shown in the following calculations. Also, the following figures show the dimensions of the two JFET's designed.

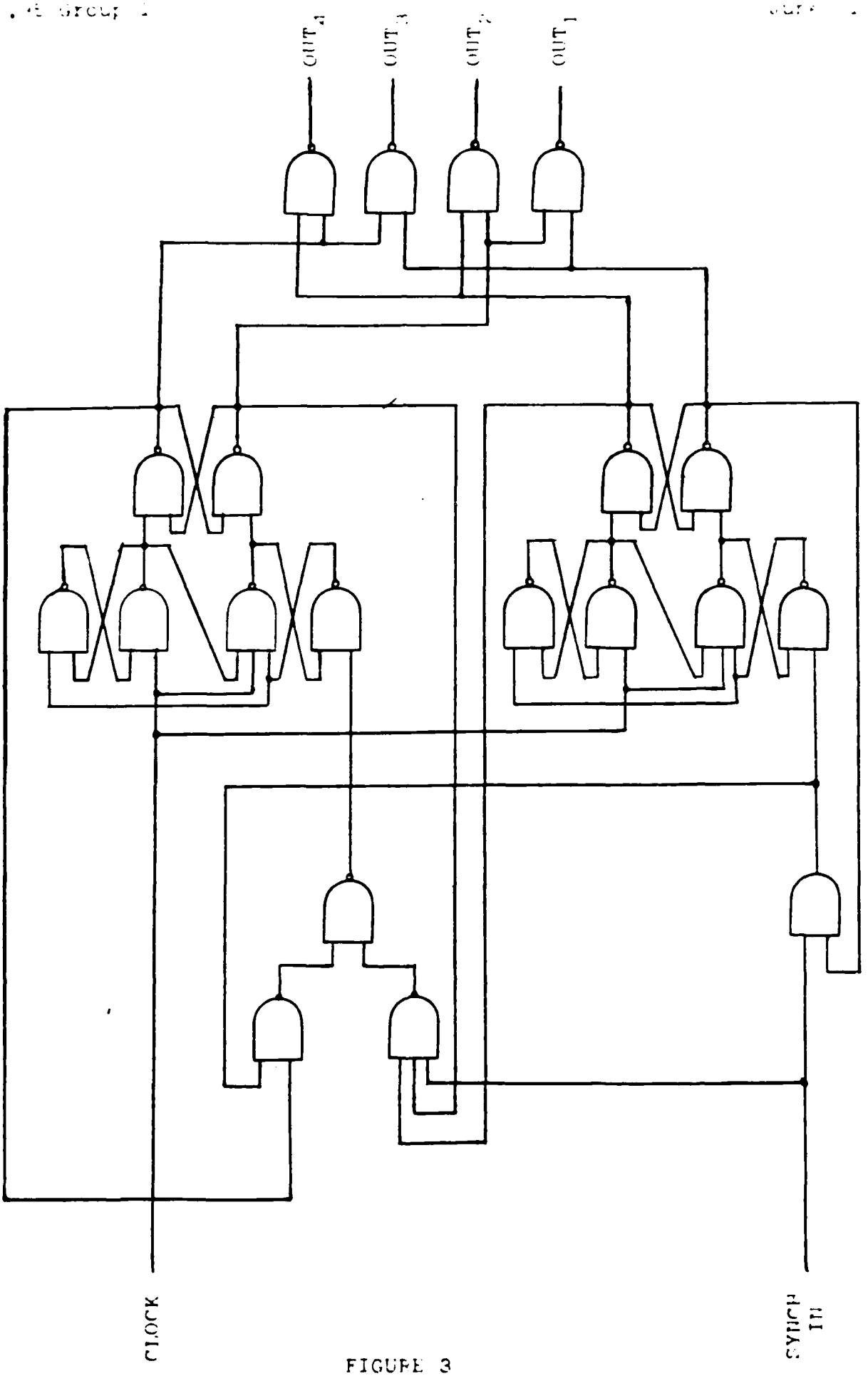
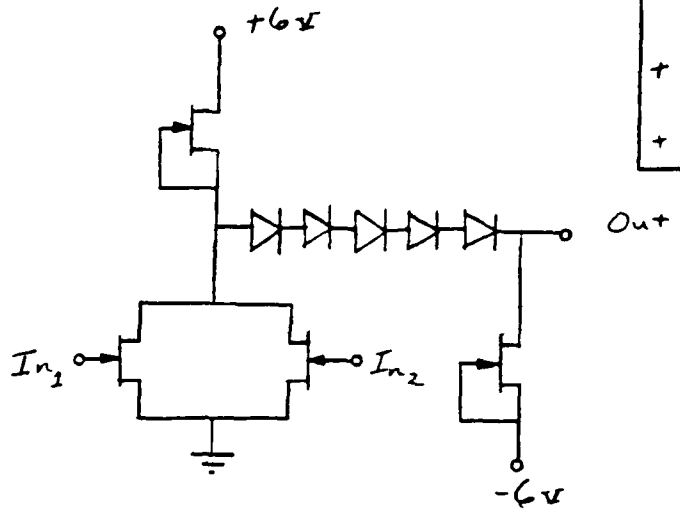


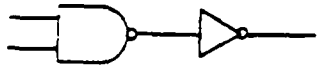
FIGURE 3

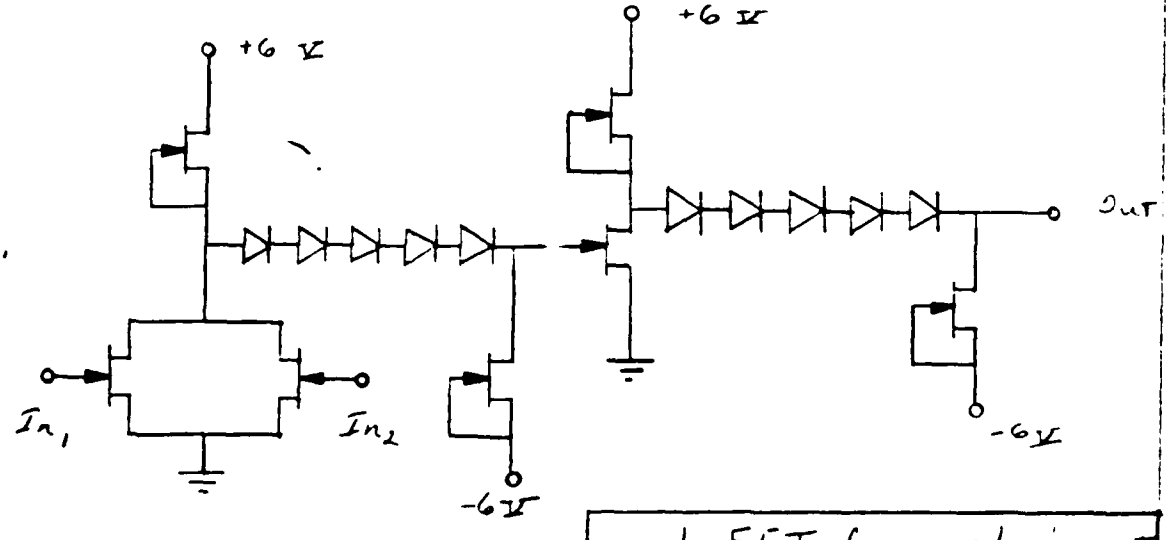
NAND



1 FET for each input
+ 2 FETs for Loads
+ 5 Diodes

AND



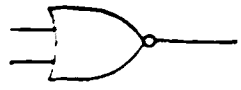


1 FET for each input
+ 1 FET for inverter input
+ 4 FETs for Loads
+ 10 Diodes

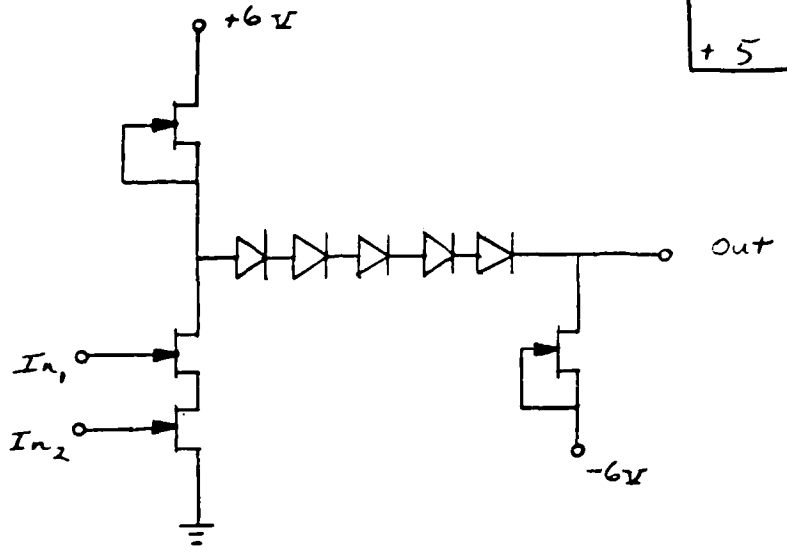
FIGURE 4

Logic Gate Implementation
Using n-channel JFETs

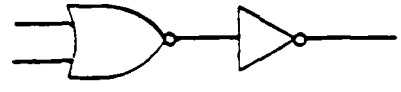
NOR

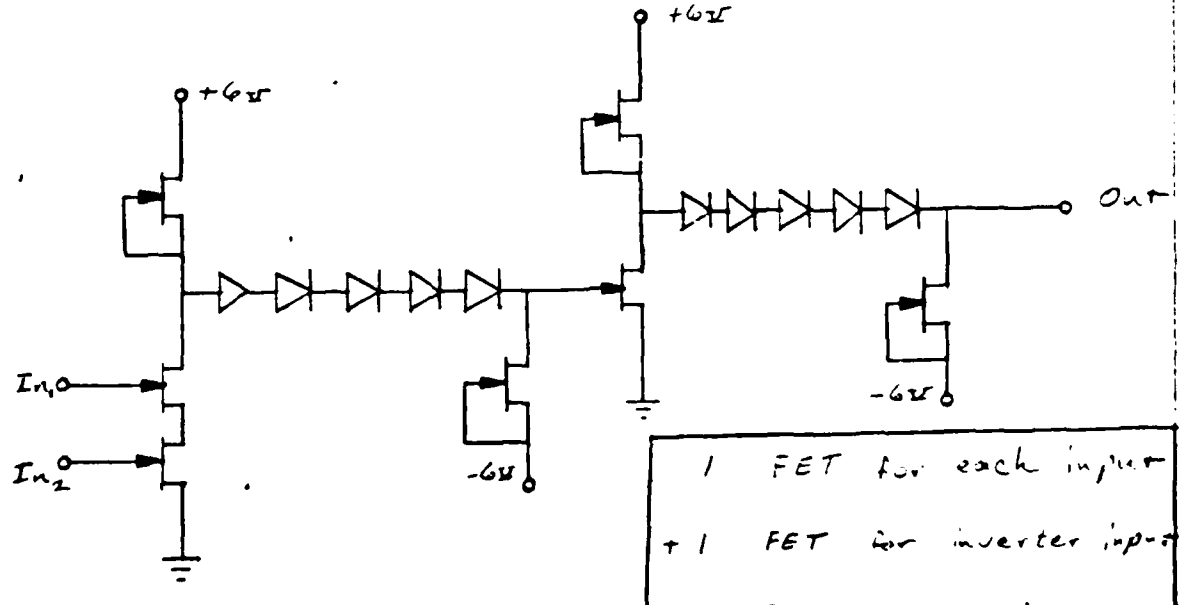


1 FET for each input
+ 2 FETs for loads
+ 5 Diodes



OR





1 FET for each input
+ 1 FET for inverter input
+ 4 FETs for Loads
+ 5 Diodes

FIGURE 5

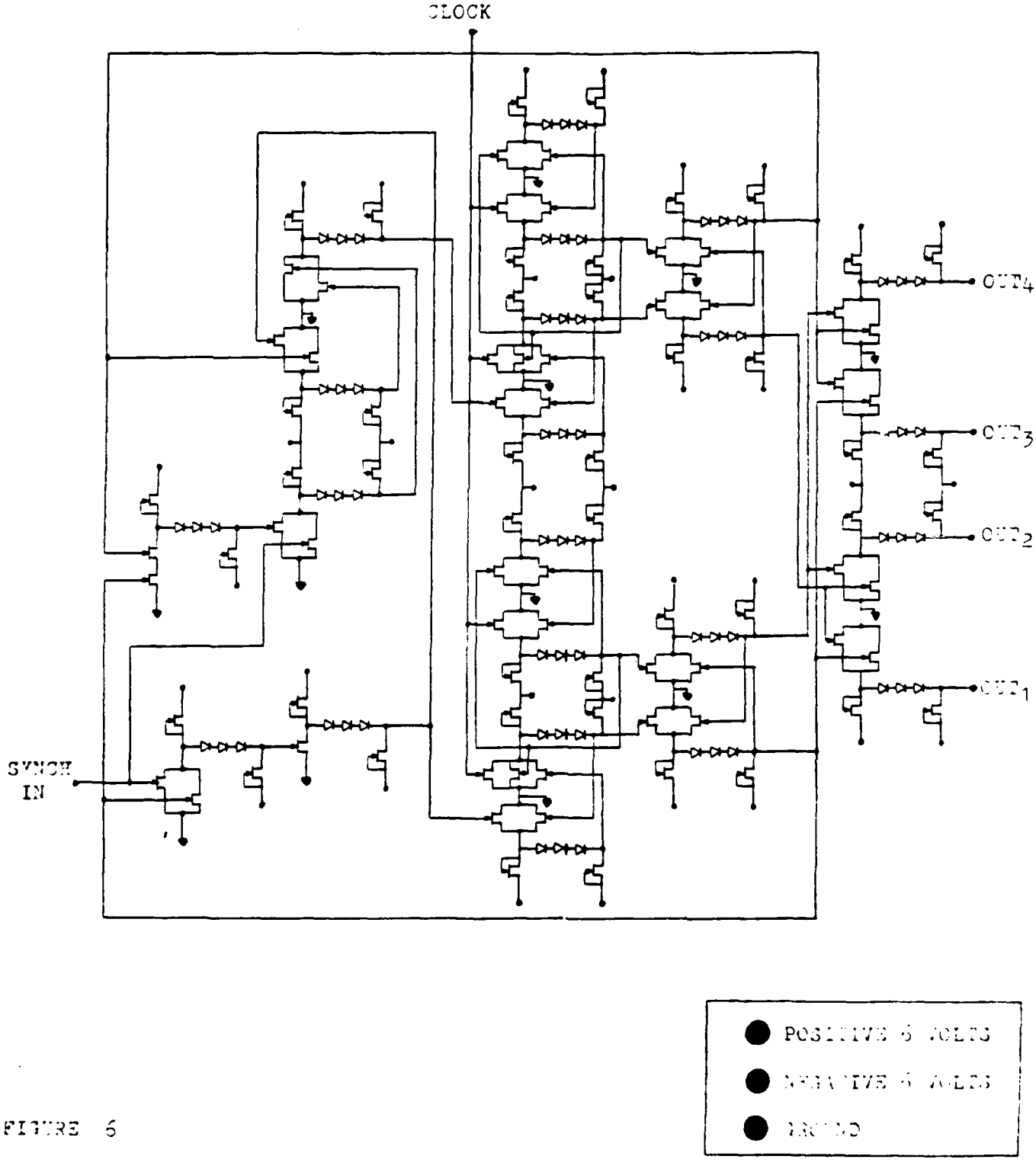


FIGURE 6

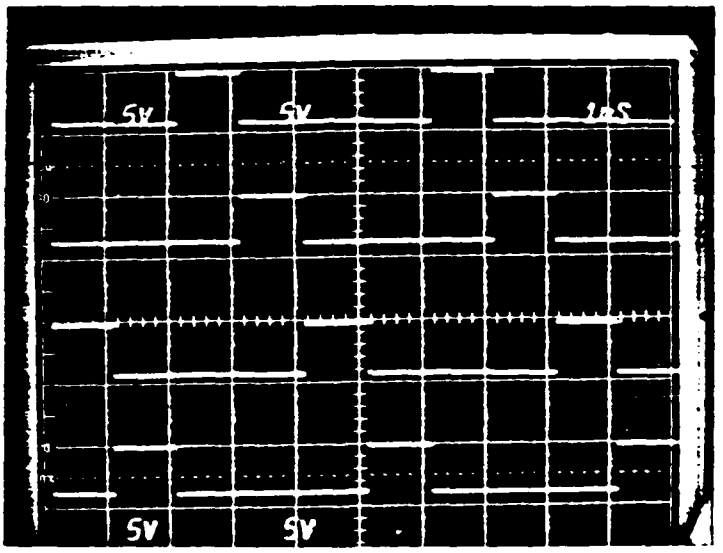
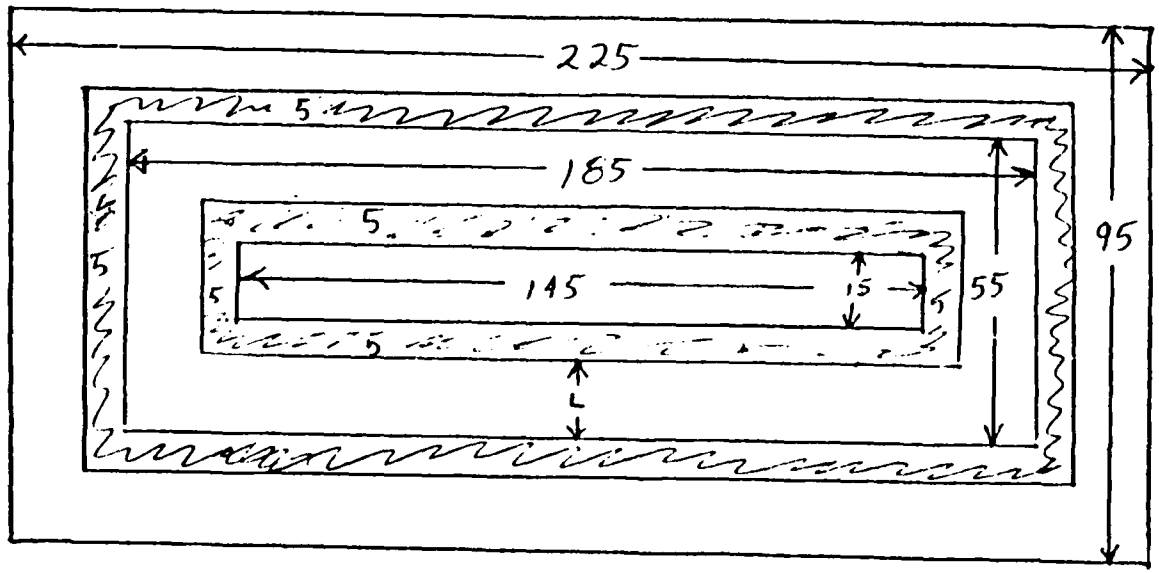
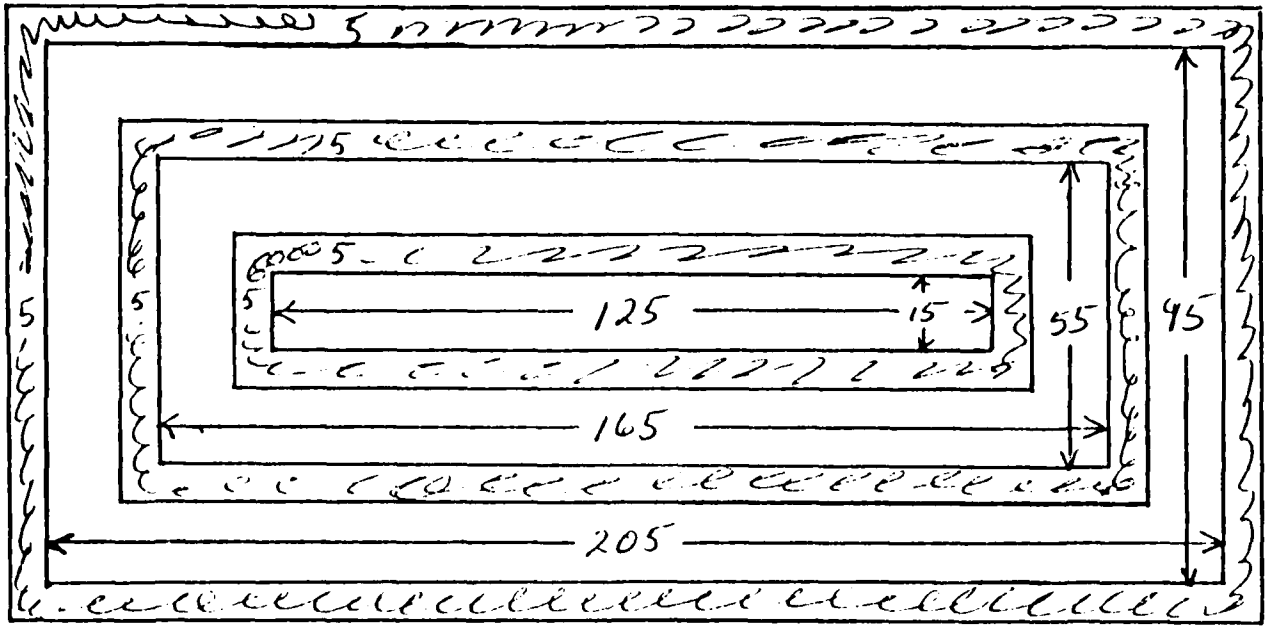


FIGURE 7



JFET For Upper Load and Switches

FIGURE 8



JFET For Lower Load

FIGURE 9

JFET DESIGN

STARTING WITH THE FOLLOWING EQUATION:

$$V_P = -\frac{d^2 e N_D}{2k} + \Phi_B .$$

SOLVING FOR d (CHANNEL DEPTH) WITH A DESIRED PINCH-OFF VOLTAGE (V_P) OF 1.5 VOLTS AND A BUILT-IN VOLTAGE (Φ_B) OF .8 VOLTS

$$d = \sqrt{\frac{2k(V_P + \Phi_B)}{e N_D}}$$

WHERE: $k = \epsilon_s \epsilon_o = 11.8\,\epsilon_o$
$= 1.045 \times 10^{-12}$

$e = 1.6 \times 10^{-19}$

$N_D = 5 \times 10^{15}\ cm^{-3}$

$$d = \sqrt{\frac{2(1.045\times10^{-12})(1.5+.8)}{(1.6\times10^{-19})(5\times10^{15})}}$$

$d = 7.75 \times 10^{-5}$ cm

$\boxed{d = .775\ \mu m}$

NEXT, THE FOLLOWING EQUATION IS USED TO OBTAIN THE ON-RESISTANCE (R_{ON}) OF THE CHANNEL:

$$R_{ON} = \frac{1}{e \mu_n N_D} \cdot \frac{L}{dZ} \qquad \text{WHERE } \rho = \frac{1}{e \mu_n N_D}$$

L = CHANNEL LENGTH

Z = CHANNEL WIDTH

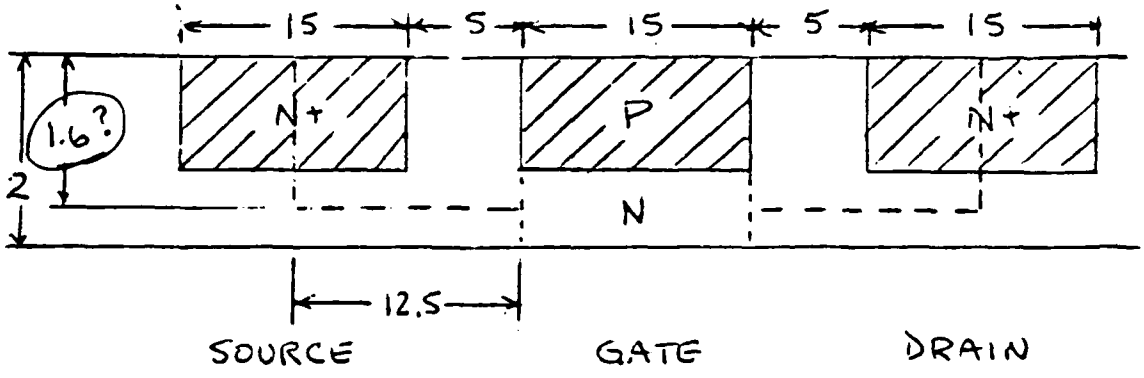
$$\therefore\ R_{ON} = \frac{\rho L}{dZ}$$

$$R_{ON} = \frac{(.9 \times 10^4\ \Omega\text{-}\mu m)(15\ \mu m)}{(.78\ \mu m)(420\ \mu m)}$$

[UPPER LOAD & SWITCH]

$$\boxed{R_{ON} = 412\ \Omega}$$

SIMILARLY, THE SOURCE AND DRAIN SERIES RESISTANCE IS SOLVED FOR USING THE SAME EQUATION AND MAKING SOME APPROXIMATIONS. LOOKING AT THE CROSS-SECTION OF THE SOURCE, GATE, AND DRAIN THE CURRENT PATH LENGTH CAN BE APPROXIMATED AS FOLLOWS:



$$R_S = \frac{\rho\, l_S}{h_S\, Z_S}$$

$$R_S = \frac{(.9 \times 10^4\ \Omega\text{-}\mu m)(12.5\ \mu m)}{(1.6\ \mu m)(360\ \mu m)}$$

$$\boxed{R_S = 195\ \Omega}$$

$$R_D = \frac{\rho\, l_D}{h_D\, Z_D}$$

$$R_D = \frac{(.9 \times 10^4\ \Omega\text{-}\mu m)(12.5\ \mu m)}{(1.6\ \mu m)(450\ \mu m)}$$

$\boxed{R_D = 147\ \Omega}$

THE TOTAL ON-RESISTANCE OF THE DEVICE IS:

$$R_{ON\,total} = R_{ON} + R_S + R_D$$

$$R_{ON\,total} = 412 + 195 + 147$$

$$\boxed{R_{ON\,total} = 754\ \Omega}$$

[UPPER LOAD & SWITCH]

SOLVING FOR THE SATURATION CURRENT USING THE FOLLOWING EQUATION:

$$I_{Dsat} = G_o \left\{ \left[\frac{2}{3} \sqrt{\frac{2k}{eN_D d^2} (\phi_B - V_G)} - 1 \right] (\phi_B - V_G) + \frac{1}{3} \frac{eN_D d^2}{2K} \right\}$$

WHERE: $G_o = \frac{1}{R_{ON}}$

& $V_G = 0\ V$

& $\cancel{\ast} = \frac{2k}{eN_D d^2} = 2.3$

$$\therefore I_{Dsat} = \frac{1}{R_{ON}} \left\{ \left[\frac{2}{3} \sqrt{\frac{\phi_B}{\cancel{\ast}}} - 1 \right] \phi_B + \frac{1}{3} \cancel{\ast_P} \right\}$$

$$I_{Dsat} = \frac{1}{412} \left\{ \left[\frac{2}{3} \sqrt{\frac{.8}{2.3}} - 1 \right] .8 + \frac{1}{3}(2.3) \right\}$$

$$I_{Dsat} = .68\ mA$$

[UPPER LOAD & SWITCH]

USING THE CRITERIA THAT THE LOWER LOAD SATURATIO CURRENT IS 10% LESS THAN THE UPPER LOAD SATURATION CURRENT, AND SOLVING FOR THE ON-RESISTANCE OF THE LOWER LOAD.

$$I_{Dsat_l} = I_{Dsat_u} - .1\, I_{Dsat_u} \qquad \text{[LOWER LOAD]}$$

$$I_{Dsat_l} = .68 - .068$$

$$\boxed{I_{Dsat_l} = .612 \text{ mA}}$$

$$R_{ON_l} = \frac{1}{I_{Dsat_l}} \left\{ \left[\frac{2}{3} \sqrt{\frac{\Phi_B - V_o}{\cancel{\Phi_B}}} - 1 \right] (\Phi_B - V_o) + \frac{1}{3} \cancel{\Phi_B} \right\}$$

$$R_{ON_l} = \frac{1}{.612} \left[.2812 \right]$$

$$\boxed{R_{ON_l} = 458\ \Omega}$$

$$R_{S_l} = \frac{\rho\, l_S}{h_S Z_S} = \frac{(.9 \times 10^4\ \Omega\text{-}\mu m)(12.5\ \mu m)}{(1.6\ \mu m)(320\ \mu m)}$$

$$\boxed{R_{S_l} = 220\ \Omega}$$

$$R_{D_l} = \frac{\rho\, l_D}{h_D Z_D} = \frac{(.9 \times 10^4\ \Omega\text{-}\mu m)(12.5\ \mu m)}{(1.6\ \mu m)(440\ \mu m)}$$

$$\boxed{R_{D_l} = 176\ \Omega}$$

$$R_{ON\ total_l} = 458 + 220 + 176$$

$$\boxed{R_{ON\ total_l} = 854\ \Omega} \qquad \text{[LOWER LOAD]}$$

FOLLOWING ARE PLOTS OF THE CHARACTERISTICS AS CALCULATED ABOVE. THE SLOPE IN THE SATURATION REGION WAS CHOSEN TO ALLOW A FOUR VOLT SWING WITH A 10% DIFFERENCE IN THE SATURATION CURRENT OF THE TWO DEVICES. THIS SLOPE TURNED OUT TO BE .02 $^{mA}/_{V}$ (FIG. 3). THE TWO REMAINING PLOTS SHOW THE EFFECT A CHANGE IN THE SLOPE IN THE SATURATION REGION WILL HAVE ON THE VOLTAGE SWING, HOLDING ALL OTHER PARAMETERS CONSTANT.

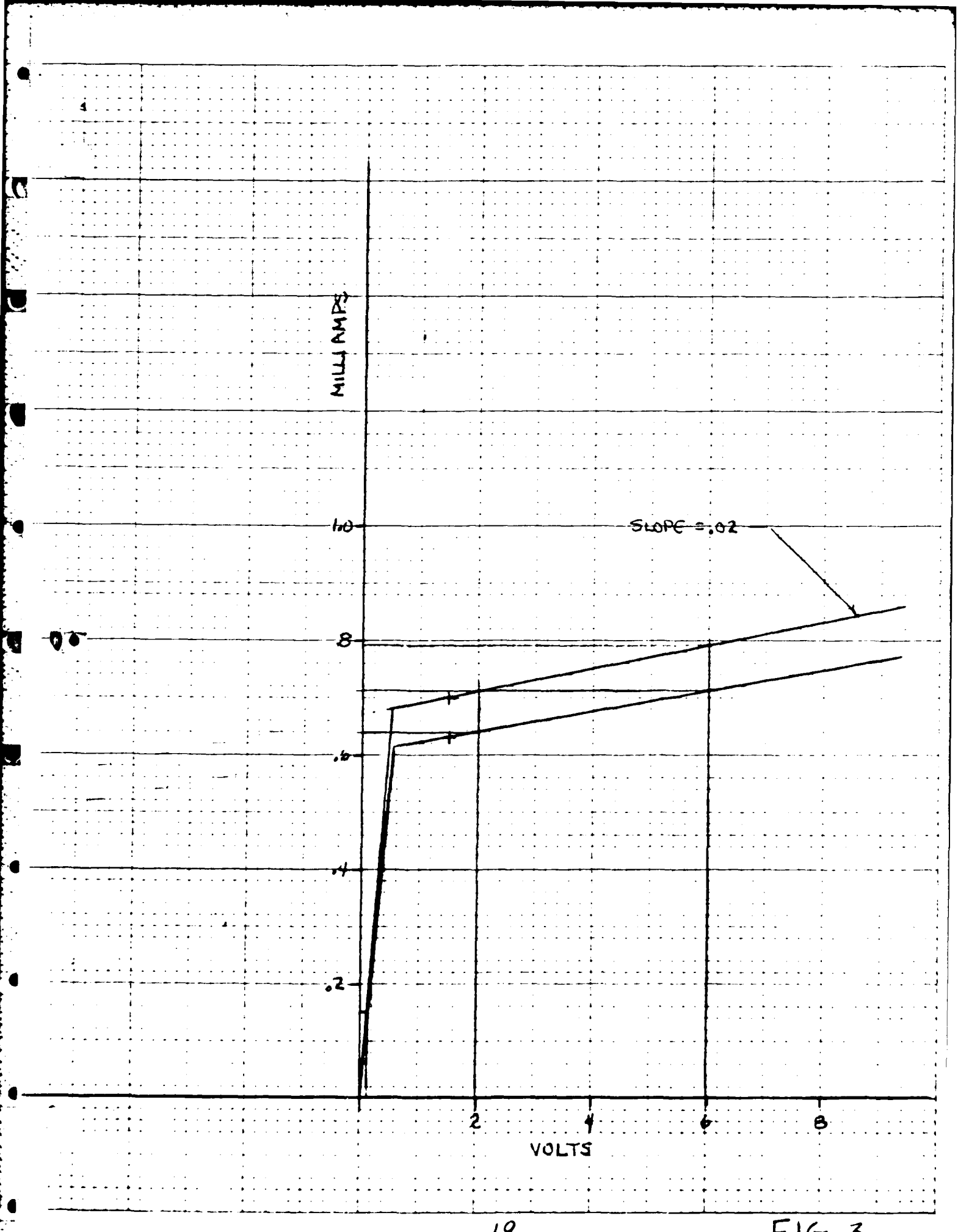


FIG 3

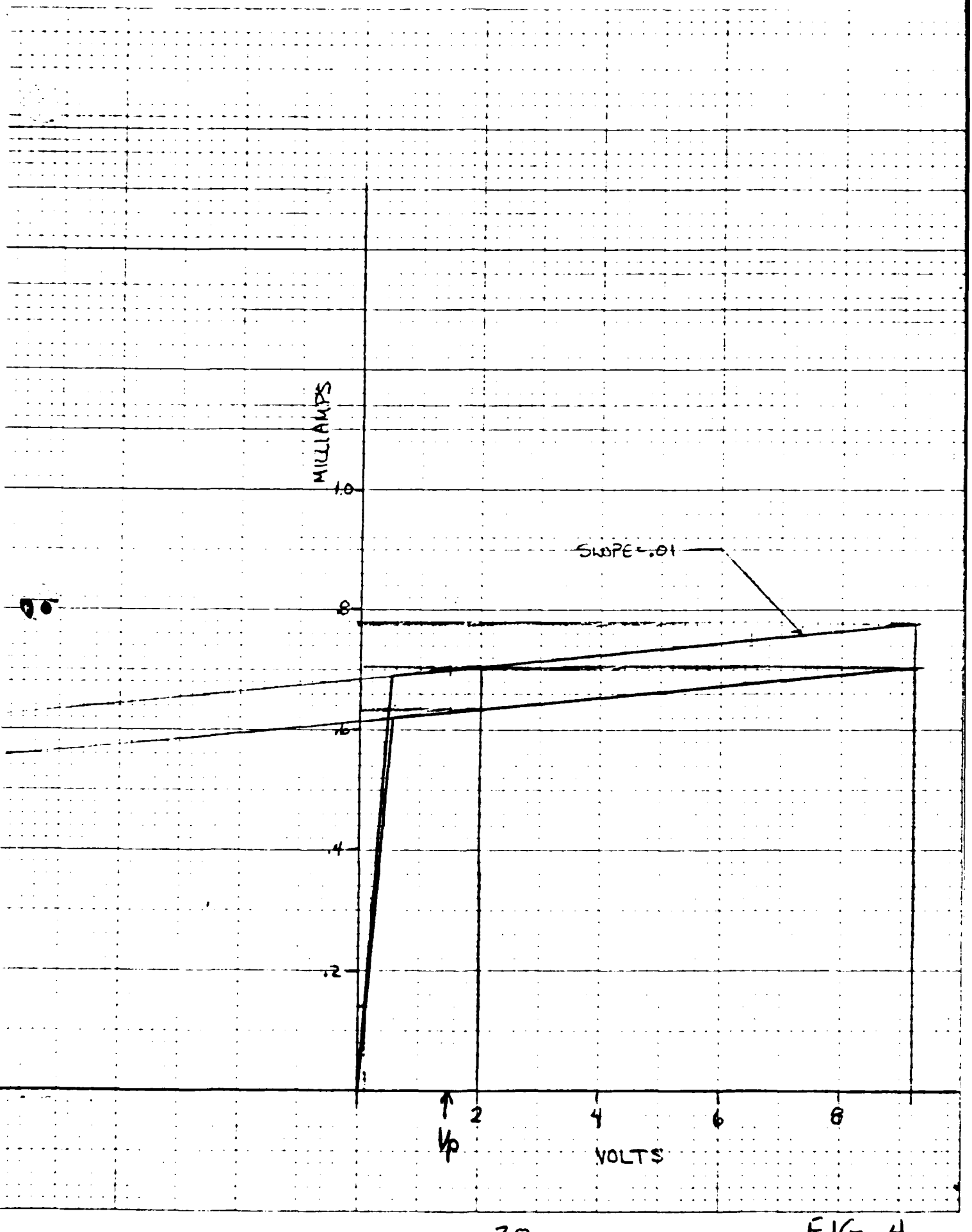


FIG. 4

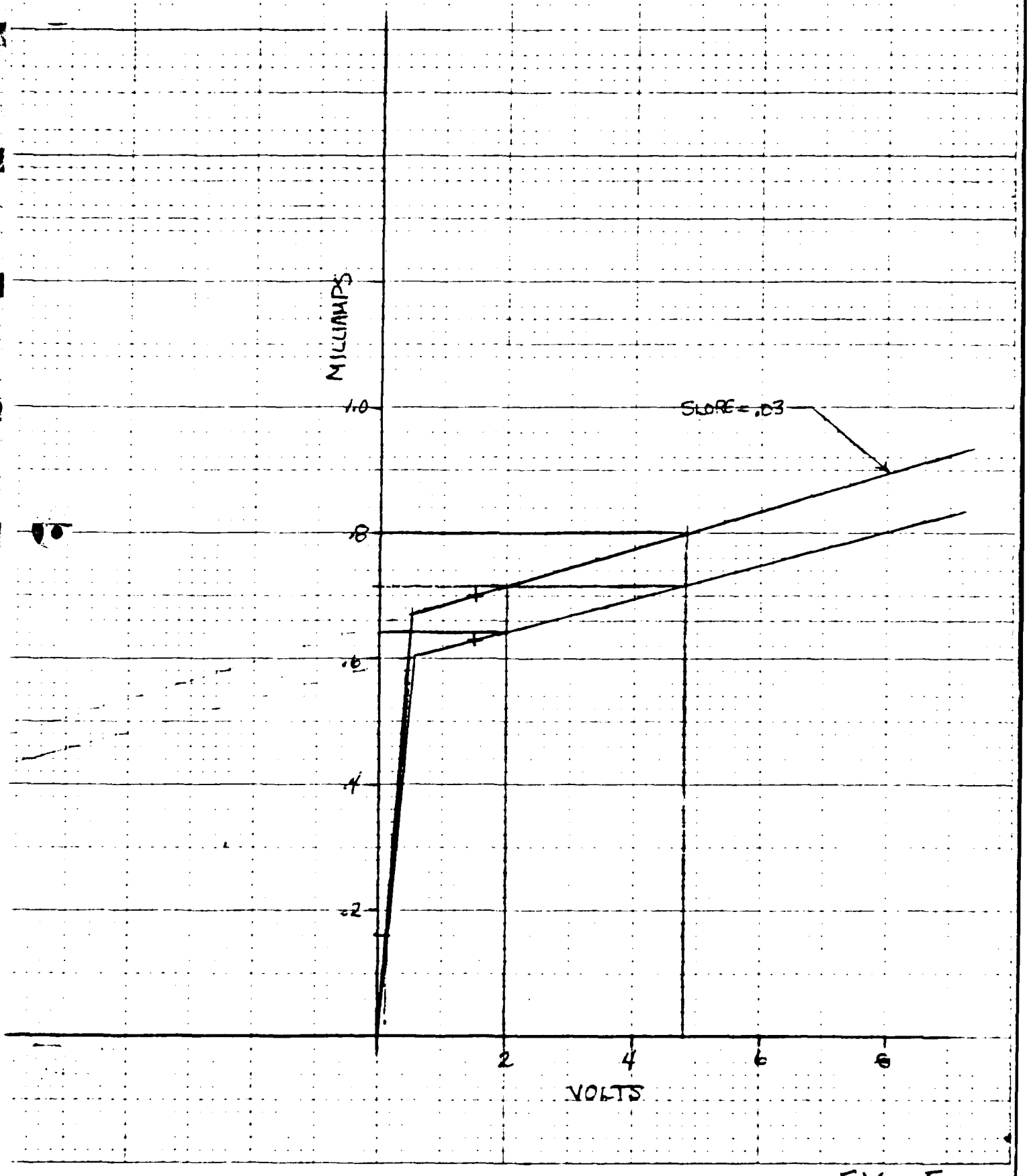


FIG. 5.

DEVELOPMENT OF THE "PG" PROGRAM

The development of pattern generator programs for this project deals with the two following subjects: 1) The circuit description, and 2) A modular design. Once both these items have been explored, the development of the entire AFIT Array becomes simpler except for modifications and development of the modules. All the modules in this project are dependent on each other throughout the entire project. This type of dependence insures that each module is kept within its outer boundaries along with any special needs that may develop do to design changes or requirement changes during the course of this design project.

1) CIRCUIT DESCRIPTION

The "brain" chip project circuitry is based on the NAND gate design. At present, a two-input NAND gate as designed is shown in Figure 1 below.

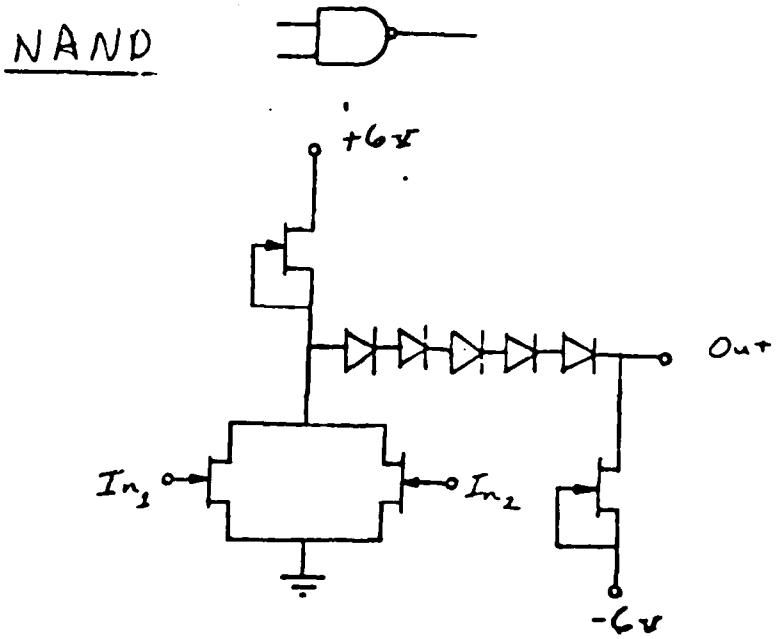


FIGURE 1 NAND Gate Design

This design uses one upper load JFET, two driver JFET's and one lower load JFET. Along with this design are five diodes placed between the output of the upper load JFET and the lower load JFET.

The overall design at this point in time deals with the JFET design developed by Lt. Tatman, along with the JFET design developed by my team partners. The diode design was agreed upon after many hours of work. All the design parameters are shown in the next three figures. From the design parameters shown there, along with the circuitry shown in figure 1, a two input Nand gate could be created using PG.

The number of diodes needed for each gate was also determined by the voltage drop required between the upper load FET and lower load FET. A complete diagram of the two input Nand gate used in the Pattern Generater stage is also shown in figure 5.

2) MODULAR DESIGN

Once the basic two input Nand gate circuitry is complete, then a module type of design of the gate begins. The modular design here is the creation of a reproducible file, in a general sense, that can be used in many areas with only minor additional work needed. The design procedure starts with the design in figure 5 along with the design parameters shown in figures 2, 3, and 4.

The modules, as designed, depend upon many factors that need to be present before the module can be implemented.

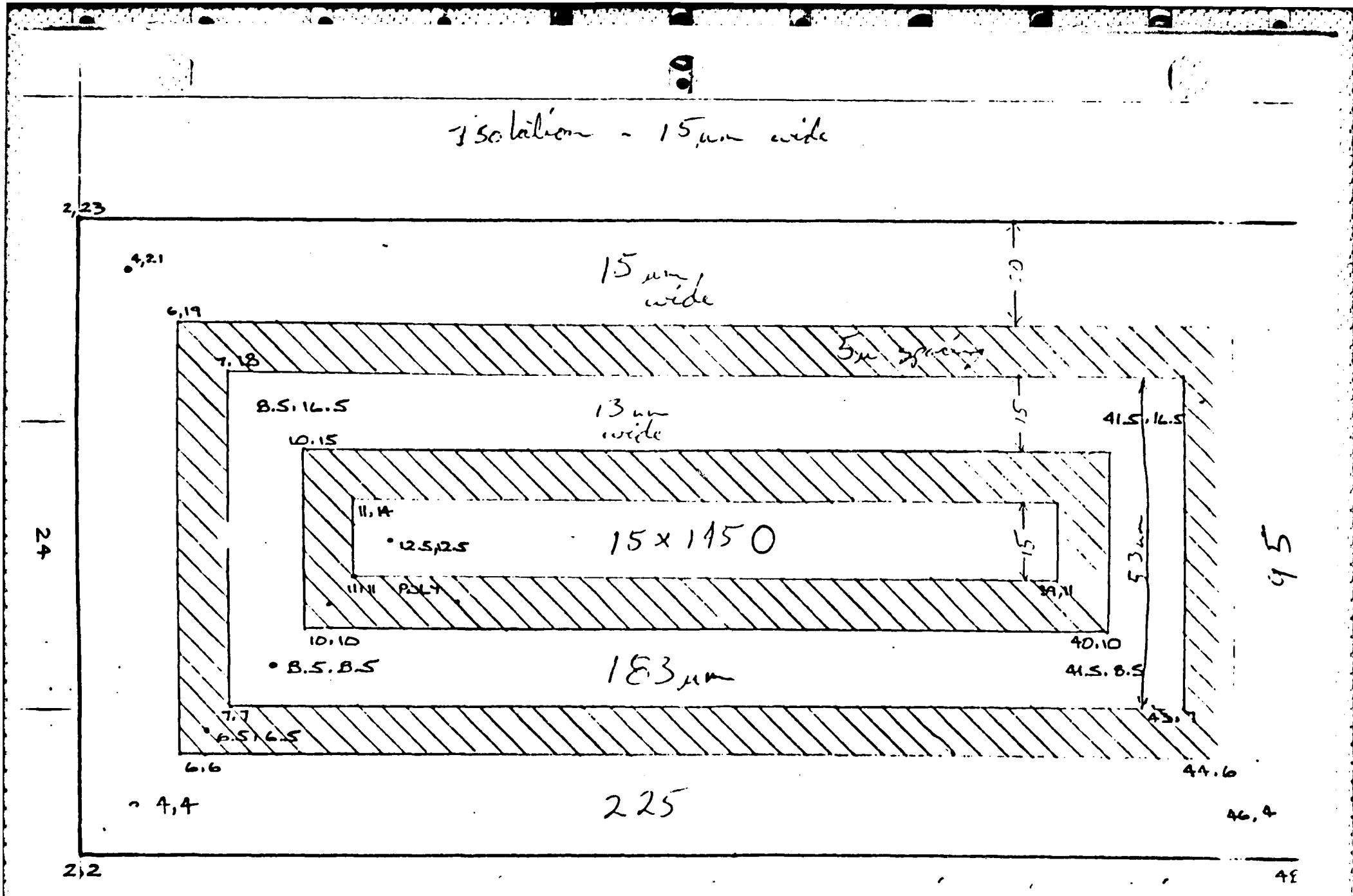


Figure 2. CCD Design for Paper Load and Drivers

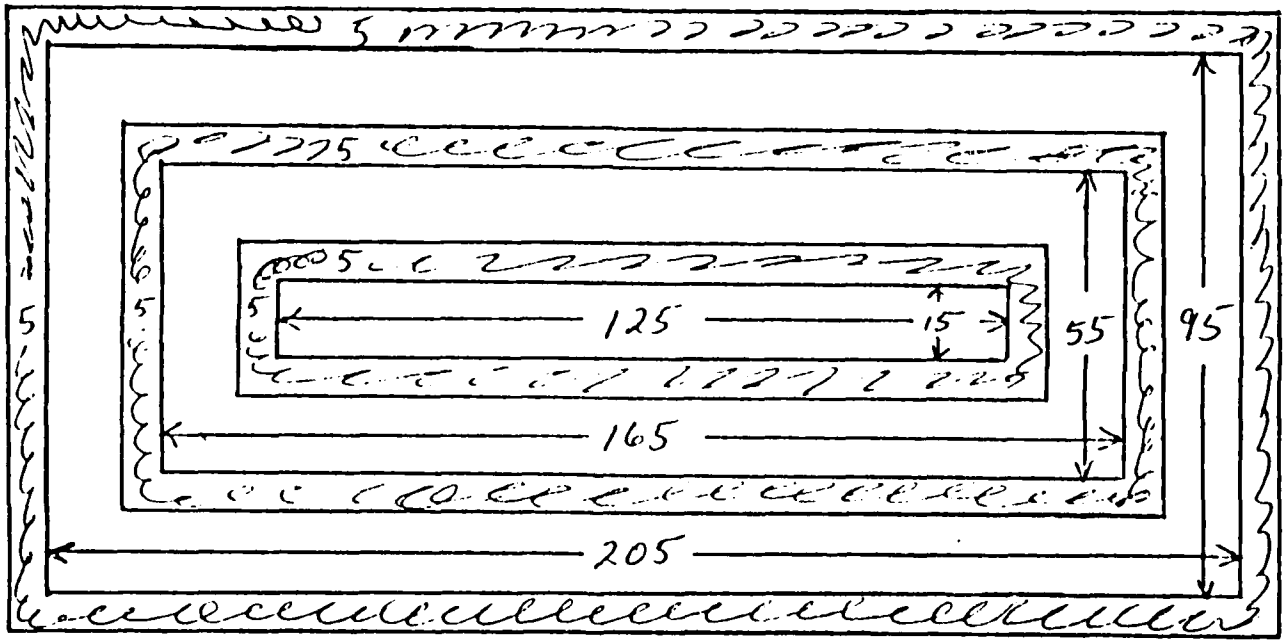


Figure 3. PCT Design for the Lower Load

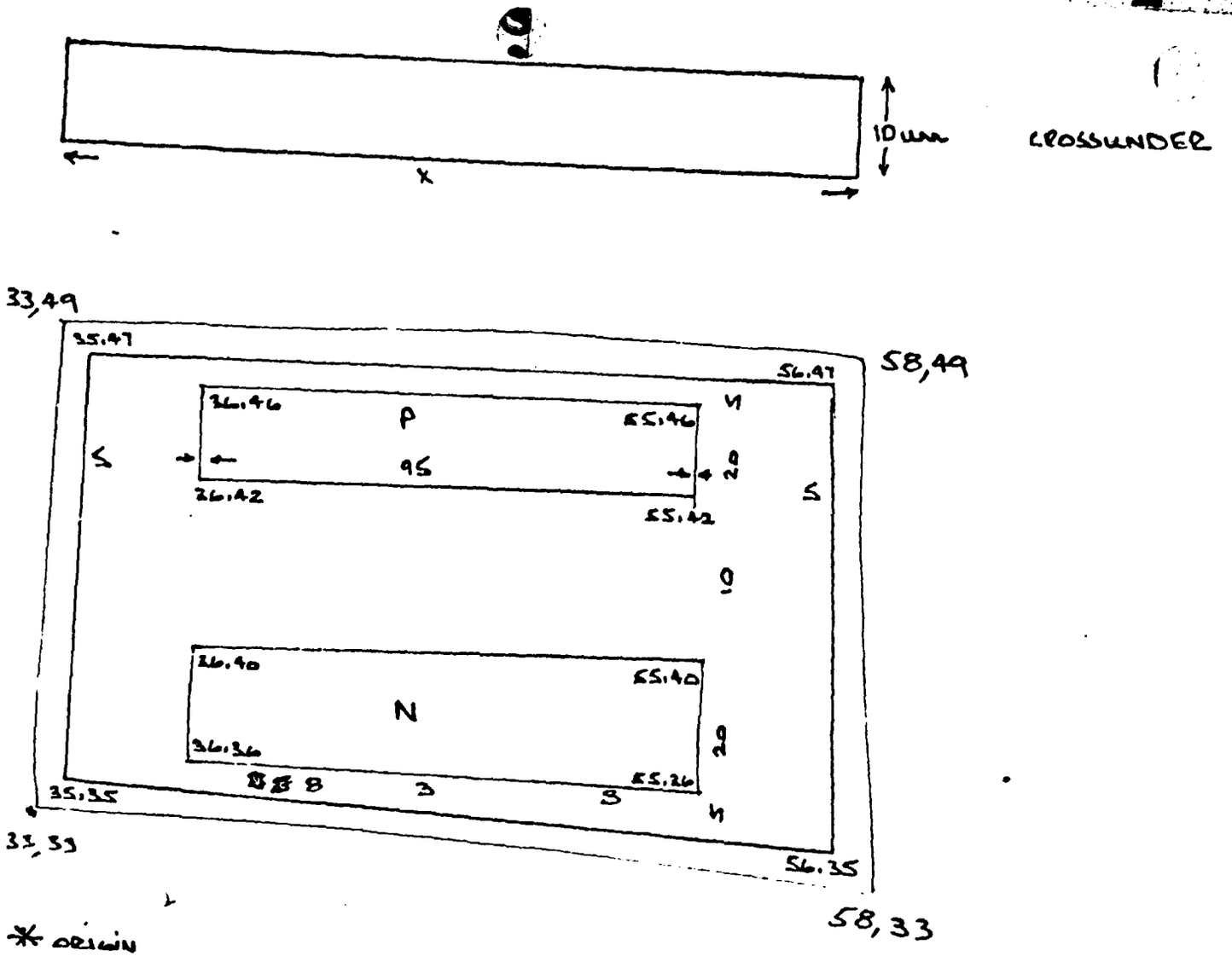


Figure 4. Diode Design and Crossunder Design

The first bits of information needed are:

1) Project Project Name,
2) Plot, optional;
3) Sort, optional;
4) Scale Factor, and
5) Chipsize

The scale factor used in this program is specifically in "mils", where our line widths are specified in microns. Therefore, a conversion had to be made in order to have line widths that were in microns. The scale factor used in programs are based on a five micron line width. Along with the scale factor is the chipsize which is also specified in microns.

The second bit of information needed for this modular design is:

1) The Origin statement, and
2) The module.

The origin statement establishes the correct position or positions, whichever the case may be, for the module to be created. The modules contain information dealing with the creation of the isolation tubs, the gate and crossunder connections, the drain and source connections, the opening of the contact areas, the metalization information, and lastly the contact window information. An example of the creation of a two input NAND gate is shown below in part three.

3) DESIGN OF A NAND GATE

A. Isolation Layer

The isolation layer, being the first, is important because all future layers are st within the boundaries of the isolation layer. The isolation tubs are created by using Path and Poly statements. Supported by PG, these statements must follow the design parameters set beforehand. The file used to do this is the NAND1 file listed in Appendix D of this report.

B. The Gate Layer and Crossunders

Once the isolation layer has been set, the gate contact points are layed in. At this time, an important point must be made. The numbers presented herein take into account both the isolation diffusion and the required layer spacing. An example of the file used to get the job done is Cellfile Gate1 listed in Appendix D of this report.

C. The Drain-Source Layer

The third layer, the drain-source layer, is set once the gate layer sets in place. The drain-source layer also includes the N-diffusion contact for the diodes in the NAND gate design. The file used for this layer is the DRS1 file listed in Appendix D of this report.

D. Opening of the Metal Contact Layer

The fourth layer is intended to open up metalization contacts through the silicon dioxide layer. Therefore a combination of the above two files must be used. One

important factor also must be addressed, the metalization layer. Before the fourth layer can be designed, the metal contacts must be looked at so that a problem of metal in a non-design area can be avoided. Therefore, design spaces must be incorporated into the fourth layer that are not present in the previous two layers. The required files for the fourth layer are GDS1 and DDLAYA which are listed in Appendix D of this report.

E. The Metalization Layer

The fifth layer is designed to connect the proposed NAND gates together along with the design areas opened by the fourth layer. This layer is the most complex and demanding layer in the entire development phase of the "brain" chip. The required file needed for this layer is METALAY1.

F. The Contact Window Layer

The sixth layer is not used in the development of the NAND gate but is used to open up contacts for the wire bonds that will be used between the chip and the outside world. These contact openings come under the SQ files.

```
[illegible]

[illegible]  0, 0 : 50, 0 : .59055
[illegible]  50, 0 : 50, 25 : .59055
[illegible]  50, 25 : [illegible] : .59055
[illegible]  0, 25 : 0, 0 : .59055

[illegible]  33, 33 : 58, 33 : .59055
[illegible]  58, 33 : 58, 47 : .59055
[illegible]  58, 47 : 33, 47
[illegible]  33, 47 : 33, 33

[illegible]  33, 57 : 58, 57 : .59055
[illegible]  58, 57 : 58, 73 : .59055
[illegible]  58, 73 : 33, 73
[illegible]  33, 73 : 33, 57

[illegible]  0, 57 : 25, 57 : .59055
[illegible]  25, 57 : 25, 73 : .59055
[illegible]  25, 73 : 0, 73
[illegible]  0, 73 : 0, 57

[illegible]  0, 83 : 25, 83 : .59055
[illegible]  25, 83 : 25, 183 : .59055
[illegible]  25, 183 : 0, 183
[illegible]  0, 183 : 0, 83
[illegible]  0, 133 : 25, 133

[illegible]  33, 83 : 58, 83 : .59055
[illegible]  58, 83 : 58, 100
[illegible]  58, 100 : 33, 100
[illegible]  33, 100 : 33, 83

[illegible]  33, 108 : 58, 108 : .59055
[illegible]  58, 108 : 58, 125
[illegible]  58, 125 : 33, 125
[illegible]  33, 125 : 33, 108

[illegible]  33, 133 : 58, 133 : .59055
[illegible]  58, 133 : 58, 183
[illegible]  58, 183 : 33, 183
[illegible]  33, 183 : 33, 133
```

Appendix D 1: NAND1 Design

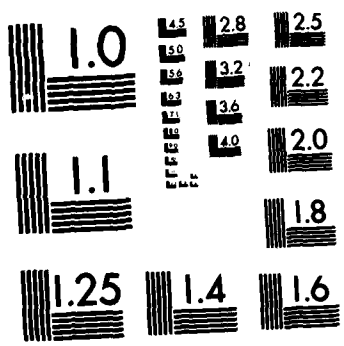
AD-A124 878 THE FIRST CORTICAL IMPLANT OF A SEMICONDUCTOR MULTIELECTRODE ARRAY: ELECT..(U) AIR FORCE INST OF TECH WRIGHT-PATTERSON AFB OH SCHOOL OF ENGI.. 3/3

UNCLASSIFIED R W HENSLEY ET AL. DEC 82 AFIT/GE/EE/82D-29 F/G 6/16 NL

END

FILMED

DTIC



```
      [illegible] : .59055
      [illegible] : [illegible] 16.5
      [illegible] : [illegible] 16.5
    : 8.5, 16.5 : 8.5, 8.5

    : 8.5, 91.5 : 16.5, 91.5 : .59055
    : 16.5, 91.5 : 16.5, 124.5
path 16.5, 124.5 : 8.5, 124.5
path 8.5, 124.5 : 8.5, 91.5

path 8.5, 141.5 : 16.5, 141.5 : .59055
p   h 16.5, 141.5 : 16.5, 174.5
p   h 16.5, 174.5 : 8.5, 174.5
pat : 8.5, 174.5 : 8.5, 141.5

path 41.5, 141.5 : 49.5, 141.5 : .59055
path 49.5, 141.5 : 49.5, 174.5
p th 49.5, 174.5 : 41.5, 174.5
p th 41.5, 174.5 : 41.5, 141.5

   : 36, 42 : 19, 4

   : 36, 66 : 19, 4

   : 36, 66 : 19, 4

   : 36,92 : 19, 4

   : 36, 117 : 19, 4
```

```
    . . 4.5, 4.5 : 42.5, 4.5 : .59055
        . 42.5, 4.5 : 42.5, 20.5
    . . 42.5, 20.5 : 4.5, 20.5
        . 4.5, 20.5 : 4.5, 4.5
    . . 11, 11 : 25, 3

    . . 36, 36 : 19, 4

    . . 36, 60 : 19, 4

    . . 3, 60 : 19, 4

        . 36, 80 : 19, 4

    . . 36, 111 : 19, 4

    . . 4, 87 : 21, 87 : .78740
    . . 21, 87 : 21, 129
        . 21, 129 : 4, 129
    . . 4, 129 : 4, 87
poly 11, 94 : 3, 28

    . . 4, 137 : 21, 137 : .78740
    . . 21, 137 : 21, 179
        . 21, 179 : 4, 179
    . . 4, 179 : 4, 137
        . 11, 144 : 3, 28

    . . 37, 137 : 54, 137 : .78740
    . . 54, 137 : 54, 179
    . . 54, 179 : 37, 179
        . 37, 179 : 37, 137
poly 44, 144 : 3, 28
```

: 8.5, 8.5 : 36.5, 8.5 : .59055
: 36.5, 8.5 : 36.5, 16.5
: 36.5, 16.5 : 8.5, 16.5
: 8.5, 16.5 : 8.5, 8.5

: 8.5, 91.5 : 16.5, 91.5 : .59055
: 16.5, 91.5 : 16.5, 124.5
: 8.5, 124.5 : 8.5, 91.5

: 16.5, 141.5 : 16.5, 174.5 : .59055
: 8.5, 174.5 : 8.5, 141.5

: 49.5, 141.5 : 49.5, 174.5 : .59055
: 49.5, 174.5 : 41.5, 174.5
: 41.5, 174.5 : 41.5, 141.5

/ 36, 42 : 19, 4

/ 36, 66 : 19, 4

/ 3, 66 : 19, 4

/ 36,92 : 19, 4

36, 117 : 19, 4

```
    [illegible] 4.5, 4.5 : 19.5, 4.5 : .59055
[illegible] 27.5, 4.5 : 42.5, 4.5
[illegible] 42.5, 4.5 : 42.5, 20.5
[illegible] 42.5, 20.5 : 4.5, 20.5
[illegible] 4.5, 20.5 : [illegible]
[illegible] : 4.5, 4.5
[illegible] 11, 11 : 25, 3

[illegible] 36, 36 : 19, 4

[illegible] 36, 60 : 19, 4

[illegible] 3, 60 : 19, 4

[illegible] 36, 86 : 19, 4

[illegible] 36, 111 : 19, 4

[illegible] 4, [illegible] : 21, 87 : .78740
[illegible] 21, 87 : 21, 129
[illegible] 21, 129 : 18, 129
[illegible] 7, 129 : 4, 129
[illegible] 4, 129 : 4, 113
[illegible] 4, 103 : 4, 87
[illegible] 11, 94 : 3, 28

[illegible] 4, 137 : 7, 137 : .78740
[illegible] 18, 137 : 21, 137
[illegible] 21, 137 : 21, 179
[illegible] 21, 179 : 18, 179
[illegible] 7, 179 : 4, 179
[illegible] 4, 179 : 4, 163
[illegible] 4, 153 : 4, 137
[illegible] 11, 144 : 3, 28

[illegible] 37, 137 : 40, 137 : .78740
[illegible] 51, 137 : 54, 137
[illegible] 54, 137 : 54, 179
[illegible] 54, 179 : 37, 179
[illegible] 37, 179 : 37, 163
[illegible] 37, 153 : 37, 37
[illegible] 54, 144 : 3, 28
```

APPENDIX G

The computer program presented hereafter was used to calculate the evoked response in the data. The program name is CAT for Computed Average Transient. This software was writted by an AFIT student (Ref. 25).

```
C*******************************************************************************

C     Title: CAT
C     Author: Lt Allen
C     Date: Oct 82

C     Function:
C        This program performs a computer averaged transient on a signal
C        data file by comparison to a strobe data file. Whenever a large
C        positive transition occurs in the strobe data file, the signal
C        data file is overlapped and summed. The resulting data file is
C        scaled to a maximum value of unity.

C     Compile command:
C        FORTRAN CAT

C     Load command:
C        RLDR/P CAT INFILE TOFILE STATUS FILCHC @FLIB@

C     Environment:
C        This is a Fortran V program that has been designed to run on
C        a mapped-RDOS Eclpise S/250 minicomputer.

C*******************************************************************************

      INTEGER FILE1(7),FILE2(7),ISTART,INUM,FILE3(7)
      INTEGER BLKS,BYTS,KEEP,FIRST,YES,NO
      REAL DATA(128),THRES(128),SUMS(512),LIMIT,DIFF,MAX,OFF

      NO=1
      YES=0
      ACCEPT "<CR>
     *Enter the signal data filename:"
      READ(11,1) FILE1(1)
 1    FORMAT(S13)

      ACCEPT "
     *   starting block (the first block is one):",ISTART
      ISTART=ISTART-1
      ACCEPT "
     *,  number of blocks:",INUM  ;each data block contains 512 bytes
                                  ;which corresponds to 128 real numbers

      ACCEPT "<CR>
     *Enter the strobe data filename:"
      READ(11,1) FILE2(1)

      ACCEPT "
     *   offset factor: ",OFF  ;the offset factor is added to the strobe
                               ;data file before its absolute value is
                               ;taken (refer to line 12)

      ACCEPT "
     *   transition magnitude:",LIMIT   ;when a positive transition of
```

```
                                    ;the magnitude LIMIT occurs in the
                                    ;absolute value of the strobe data
                                    ;file, the signal data file begins
                                    ;overlapping
      LIMIT=ABS(LIMIT)

      CALL STATUS (FILE1,BLKS,BYTS)   ;verify that the signal and strobe
      IF ((INUM+ISTART).GT.BLKS)      ;files are as large as specified
     *CALL ERROR("signal data file not this large")
      CALL STATUS (FILE2,BLKS,BYTS)
      IF ((INUM+ISTART).GT.BLKS)
     *CALL ERROR("strobe data file not this large")
      CALL FILCHC (FILE1,FILE2)   ;verify that the signal and strobe
                                  ;filenames are not identical
C
C     The SUMS array is used to hold the CAT results. This array is
C     initialized to zeros.
C
      DO 10 I=1,512
      SUMS(I)=0.
 10   CONTINUE

C*************************************************************************

      FIRST=ISTART
      KEEP=NO   ;data is ignored until the first transition is found

 20   CALL INFILE(FILE1,FIRST,1,DATA,128)  ;the signal and strobe data
      CALL INFILE(FILE2,FIRST,1,THRES,128) ;are retrieved in one block
                                           ;sections

      TYPE "   --> ",FIRST+1," <--"

      DO 13 I=1,128
 12   THRES(I)=ABS(OFF+THRES(I))
 13   CONTINUE

 30   I=0

 35   I=I+1

      DIFF=THRES(I+1)-THRES(I)

      IF (DIFF.LE.LIMIT) GO TO 40
      J=0
      KEEP=YES

 40   IF (KEEP.EQ.NO) GO TO 45
      J=J+1
      SUMS(J)=SUMS(J)+DATA(I)

 45   IF (I.LE.127) GO TO 35
      FIRST=FIRST+1
```

```
      IF (FIRST.LT.(ISTART+INUM)) GO TO 20

C*************************************************************************

      ACCEPT "<CR>
     *Enter the filename to receive data:"
      READ(11,1) FILE3(1)

      MAX=0.
      DO 50 I=1,512
      IF (SUMS(I).GE.MAX) MAX=SUMS(I)
 50   CONTINUE

      TYPE "<CR>
     *The maximum in the data file is ",MAX

      TYPE "<CR>
     *The data file will be automatically scaled by this amount."

      DO 55 I=1,512
      SUMS(I)=SUMS(I)/MAX
 55   CONTINUE

      CALL TOFILE(FILE3,SUMS,512)

      TYPE "<CR>
     *All Done ! <CR>"

      CALL EXIT
      END

C*************************************************************************
```

VITA

Russell William Hensley was born the son of Russell A. and Bettie J. Hensley on 13 July 1947 in Huntington, West Virginia. He graduated from Central High School in Columbus, Ohio and entered the United States Air Force in June 1965. After attending both the State College of Arkansas, in Conway, Arkansas and Ohio State University, in Columbus, Ohio, he recieved the degree Bachelor of Science in Electrical Engineering on 11 June 1976 from Ohio State University. He recieved his commision from Officer Trainaing School in October 1976 and was assigned to the Flight Dynamics Laboratory at Wright-Patterson AFB where he served as a Simulator Systems Design Engineer. He entered the School of Engineering, Air Force Institute of Technology in June 1981. He is a member of Eta Kapa Nu and Tau Beta Pi honor societies.

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Multielectrode array
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Visual evoked response (VER)

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Previous bioengineering research conducted at the Air Force Institute of Technology (AFIT) motivated the development of a multielectode array capable of extracting and recording bioelectrical signals present of the mammalian cortex. Part of the work presented here involves the total redesign and packaging of the drive circuitry necessary to operate the AFIT Array. Visual evoked response (VER), independent test circuitry and JFET compensation were

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also incorporated into the redesign. Several unique packsging techniques were developed to protect the semiconductor devices from a Cerebrospinal Fluid (CSF) (i.e. saline) environment. New encapsulation processes with polyimide enabled development of the Afit Array into a chronic cortically implantable probe. A simple nondestructive surgical procedure was developed, which permits access to visual cortex. The probe was then implanted into a laboratory beagle and bioelectrical (cortical) data were collected over a period of 19 days. VER techniques were used to test whether the biolobical data collected reflected actual brain functions. The data analysis to date clearly shows the bioelectric signals to be electronencephalographic (eeg) in orgin. Conclusions about the AFIT array encapsulation, drive system, surgical technique and data analysis are discussed. Recommendations for future research with the AFIT Array pertain to most aspects of the experiment. Futhermore, there are recommendations for additional experiments.

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